U.S.N P.E.S. College of Engineering, Mandya - 571 401 (An Autonomous Institution affiliated to VTU, Belagavi) Seventh Semester, B.E. - Electronics and Communication Engineering Semester End Examination; Jan. / Feb. - 2021 Low Power VLSI Design Time: 3 hrs Max. Marks: 100 Note: Answer FIVE full questions, selecting ONE full question from each unit. UNIT - I Explain the different sources of power dissipation. 6 1 a. Discuss with a neat energy band diagram of the MIS structure at different bias conditions. 8 b. Explain the effect of body effect and sub threshold swing in long channel MOSFET. 6 c. Explain the effects influencing threshold voltage in short channel devices. 6 2 a. Discuss the short circuit and dynamic power dissipation in CMOS. 10 b. Mention the principal of Low Power design. 4 c. UNIT - II 3 a. Discuss how the power dissipation improvement is done using various levels of 6 design abstraction? b. Explain the algorithm using first order differences for generating FIR filter output. 8 Explain with it signal flow graph Transposed Direct Form (TDF) FIR computation. 6 c. Discuss the power optimization using operation reduction and substitution method. 4 a. 10 b. Explain the FSM and combinational logic synthesis with suitable state machine 10 representation. **UNIT - III** 5 a. Write notes on;

		6	
i) Gate delay model	ii) Switching events probabilities	0	
Explain the following terms with references transistor reordering;		6	
i) Delay	ii) Power consumption	0	
Explain the ratio-logic using only nmo	s and pseudo nmos logic network.	8	
. Realize and implement NAND / AND logic and XOR / XNOR logic using CPL logic.		6	
b. Discuss how clocked logic families are faster than the static logic families by using domino logic?		6	
		0	
What are the factors influencing leak c	urrent in deep sub micrometer transistor?	8	
UNIT - IV			
Discuss the organization of RAM.		6	
Explain 6T SRAM cell operation with	circuit diagram.	8	
Discuss the latched sense amplifier with	th the help of a circuit diagram.	6	
	Explain the following terms with refere i) Delay Explain the ratio-logic using only nmo Realize and implement NAND / AND Discuss how clocked logic families domino logic? What are the factors influencing leak c Discuss the organization of RAM. Explain 6T SRAM cell operation with	Explain the following terms with references transistor reordering; i) Delay ii) Power consumption Explain the ratio-logic using only nmos and pseudo nmos logic network. Realize and implement NAND / AND logic and XOR / XNOR logic using CPL logic. Discuss how clocked logic families are faster than the static logic families by using domino logic? What are the factors influencing leak current in deep sub micrometer transistor? UNIT - IV	

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8 a.	Discuss the energy dissipation in Transistor channel using an RC model.			
b.	Explain with diagram, Adiabatic dynamic logic in CMOS inverter.	10		
UNIT - V				
9 a.	Discuss the sources of software power dissipation.	10		
b.	Describe the software power estimation at gate architectural level and bus switching activity.	10		
10 a.	Explain the software power optimization using algorithm Transformation.	10		
b.	Discuss power management for software optimization.	10		

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