



U.S.N

--	--	--	--	--	--	--	--	--	--

P.E.S. College of Engineering, Mandya - 571 401
 (An Autonomous Institution affiliated to VTU, Belagavi)
Third Semester, B.E. - Electronics and Communication Engineering
Semester End Examination; Dec. - 2019
Digital Electronic Circuits

Time: 3 hrs

Max. Marks: 100

Note: i) **PART - A** is compulsory. **Two** marks for each question.

ii) **PART - B:** Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.

Q. No.	Questions	Marks
I : PART - A		10
I a.	Draw the schematic of 2 I/P DTL NAND gate.	2
b.	List two characteristics of combinational logic circuits.	2
c.	Write excitation table for JK flip flop.	2
d.	List two advantages of synchronous counters.	2
e.	State the significance of state machine models.	2
II : PART - B		90
UNIT - I		18
1 a.	List the gate performance parameters and explain any three.	9
b.	Analyze the operation of 2 input TTL NOR gate with required schematic and table.	9
c.	Explain with a neat diagram the operation of 2 I/P CMOS AND gate.	9
UNIT - II		18
2 a.	Optimize the Boolean function: $f(a, b, c, d) = \sum m(0, 1, 3, 4, 5, 7, 12, 13, 15)$	9
b.	Using K-map, find all prime implicants, essential prime implicants and a minimal sum of products expression for $F(a, b, c, d) = \sum m(1, 4, 5, 6, 7, 12, 13, 14)$.	9
c.	Simplify using 4 variable VEM K-map $F(A, B, C, D) = \bar{A}\bar{B}C + \bar{A}BC + \bar{A}B\bar{C}D + ABCD + A\bar{B}C$	9
UNIT - III		18
3 a.	Describe the principle of operation of a 4 bit carry Look ahead adder with a block diagram.	9
b.	Construct a scheme to obtain a 5-to-32 line decoder using 74138 (3-8 line decoder).	9
c.	Realize the function $f(A, B, C) = \sum m(0, 1, 3, 5, 7)$, using i) 8:1 MUX ii) 4:1 MUX.	9
UNIT - IV		18
4 a.	Write the gate level diagram for the master slave S-R Flip Flop and describe its operation.	9
b.	What is latch? Draw the gate level schematic of D-Latch and write its timing diagram.	9
c.	Illustrate the significance of edge triggering? Analyze the working of positive edge triggered D-Flip Flop with asynchronous inputs.	9
UNIT - V		18
5 a.	Explain with neat diagram the working of universal shift register.	9
b.	Design a synchronous mod-5 Up counter using clocked JK-Flip Flop.	9
c.	Explain with a neat diagram the architecture of 8086 micro processor.	9