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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Computer Science and Engineering

Semester End Examination; March - 2021

Digital Logic Design

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: Design simplified logic circuits using Boolean equation minimization techniques.

CO2: Design the data processing circuits.

CO3: Design memory circuits.

CO4: Design shift registers and counters using flip-flops.

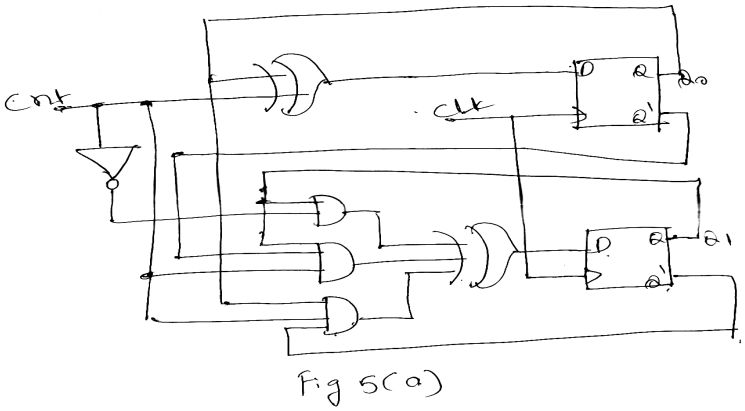
CO5: Derive state machine models for sequential circuits and write VHDL code for all logic circuits.

***Note**: I) **PART - A** is compulsory. **Two** marks for each question.*

*II) **PART - B**: Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.*

Q. No.	Questions	Marks	BLs	COs	POs
	I : PART - A	**10**			
I a.	What is the total number of minterms in the Boolean expression A + BC?	2	L1	CO1	PO1, 2, 3
b.	Design 8:1 multiplexer using 2:1 multiplexers.	2	L4	CO2	PO1, 2, 3
c.	How do you convert a JK flip-flop to T flip-flop?	2	L3	CO3	PO1, 2, 3
d.	Write the counting sequence of 4-bit Johnson counter with an initial value of 0000.	2	L2	CO4	PO1, 2, 3
e.	What is the difference between verilog full case and parallel case?	2	L1	CO5	PO1, 2, 3
	II : PART - B	**90**			
	UNIT - I	**18**			
1 a.	Give the truth table for the following function and reduce the same using Karnaugh map technique: $F(A, B, C, D) = \Sigma m\,(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$	6		CO1	PO1, 2, 3
b.	Define minterm, maxterm, negative logic and positive logic. Simplify the following function using k-map technique and implement using basic gates $F(A, B, C, D) = B'C'D' + ABD + B'CD + BC'D' + A'BCD$	12		CO1	PO1, 2, 3
c.	Simplify the following expression using tabulation method and give the circuit for essential prime implicants. $F(A, B, C, D) = \Sigma m(0, 4, 8, 10, 12, 13, 15) + d(1, 2)$	12		CO1	PO1, 2, 3
	UNIT - II	**18**			
2 a.	What is magnitude comparator? Design 4-bit comparator using logic gates.	9		CO2	PO1, 2, 3
b.	Design a combination circuit to convert; i) 3-bit binary to its 1's compliment form ii) 3-bit binary value to its gray code	9		CO2	PO1, 2, 3

Contd… 2

	c. Explain different multiplexers (4:1, 8:1, 16:1). Implement the following using 4:1 multiplexer $F(A, B, C, D) = \Sigma m(0, 2, 3, 5, 6, 7, 11, 14, 15)$	9	CO2 PO1, 2, 3
	UNIT - III	**18**	
3 a.	Explain Programmable Logic Array (PLA). Design the Boolean functions using PLA. $A = XY + XZ'$ $B = XY' + YZ + XZ'$ X Y	9	CO3 PO1, 2, 3
	b. Convert the following flip flop and draw the circuit and explain; i) SR flip flop to D flip flop ii) JK flip flop to D flip flop	9	CO3 PO1, 2, 3
	c. What is race around conditions? Explain master slave JK flip flop using NAND gate.	9	CO3 PO1, 2, 3
	UNIT - IV	**18**	
4 a.	Explain Ring counter and Johnson counter in detail.	9	CO4 PO1, 2, 3
	b. Design an asynchronous decade counter and explain with timing diagram.	9	CO4 PO1, 2, 3
	c. Design mod-6 synchronous counter using JK flip flop and implement the same.	9	CO4 PO1, 2, 3
	UNIT - V	**18**	
5 a.	Derive the state table and state and timing diagram for sequential circuit in Fig. 5(a).  Fig 5(a)	12	CO5 PO1,2,3,5
	b. Give the state synthesis table, design equation and circuit diagram for vending machine problem.	12	CO5 PO1,2,3,5
	c. Write the VHDL code for; i) T-flip flop ii) 8:1 multiplexer	6	CO5 PO1,2,3,5

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