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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

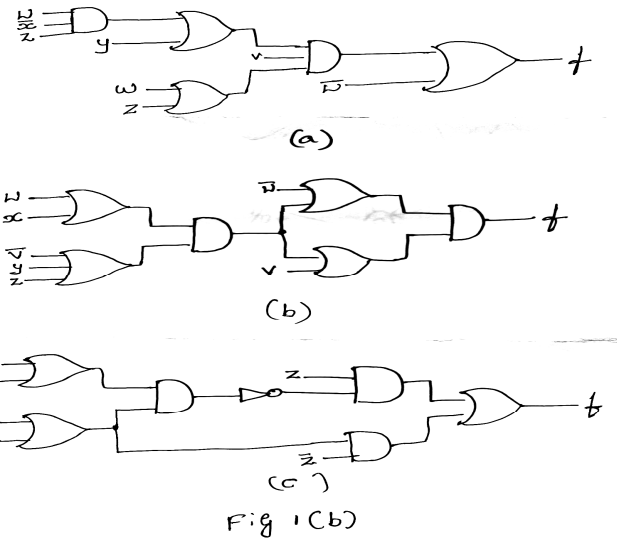
Third Semester, B.E. – Information Science and Engineering

Semester End Examination; Dec. - 2019

Digital Design

Time: 3 hrs *Max. Marks: 100*

Note: I) **PART - A** is compulsory. One question for 2 marks from each unit.
II) **PART - B**: Answer any **two** sub questions (from a, b, c) for Maximum of 18 marks from each unit.

Q. No.	Questions	Marks
	I : PART - A	**10**
I a.	Draw the logic circuit for the following equations : *i)* $Y = A\overline{B}C + ABC$ *ii)* $Y = (\overline{A} + B + C)(A + B + \overline{C})$	2
b.	Convert the following BCD numbers into their decimal equivalents : i) 100000010011 ii) 0111001001011001	2
c.	Distinguish between PLA versus PAL.	2
d.	Draw the circuit diagram and truth table of SR flip flops using NOR and NAND gates	2
e.	Write a state transition diagram of sequence detector in Moore and Mealy model.	2
	II : PART - B	**90**
	UNIT - I	**18**
1 a.	Write each to the following min term Canonical formulas in algebraic form and construct their corresponding truth tables: *i)* $f(x, y, z) = \sum m(0, 2, 4, 5, 7)$ *ii)* $f(w, x, y, z) = \sum m(1, 3, 7, 8, 9, 14, 15)$	9
b.	Write a Boolean expression for each of the logic diagram in Fig.1(b)  Fig 1(b)	9
c.	Using K-maps determine all the minimal sums and minimal products for each of the following Boolean functions. *i)* $f(w, x, y, z) = \sum m(0, 1, 6, 7, 8, 14, 15)$ *ii)* $f(w, x, y, z) = \Pi M(4, 6, 7, 8, 12, 14)$ *iii)* $f(w, x, y, z) = \overline{w}\overline{x}z + xyz + w\overline{x}z + x\overline{y}\overline{z}$	9

Contd...2

UNIT - II **18**

2 a. Realize the function $f(x, y, z) = \sum m(0, 2, 3, 5)$ using 4:1 line multiplexer. 9

b. Write and explain the parity generator and checker circuits. 9

c. Explain the construction of 4-bit carry lookahead adder. 9

UNIT - III **18**

3 a. Realize the following Boolean expression using Programming Logic Array (PLA) and Programming Array Logic (PAL) :

i) $f_1(w, x, y, z) = \sum m(2, 4, 5, 10, 12, 13, 14)$

ii) $f_2(w, x, y, z) = \sum m(2, 9, 10, 11, 13, 14, 15)$ 9

b. What is the full scale output voltage of a 6 bit binary ladder of 0 = 0 V and 1 = +10 V of an 8-bit ladder? Find the output voltage of a 6-bit binary ladder with the following inputs? 9

i) 101001 ii) 111011 iii) 110001

c. Explain the Read Only Memory diode circuits. 9

UNIT - IV **18**

4 a. Give the characteristic equation, excitation table, state diagram of SR flip flop and JK flip flop. 9

b. Illustrate how JK flip flops can be converted to SR flip flops? 9

c. With circuit diagram, explain serial in serial out and parallel in serial out shift registers. 9

UNIT - V **18**

5 a. Design an asynchronous up down counter. 9

b. Using row elimination method to reduce the state diagram as shown in Fig. 5(b).

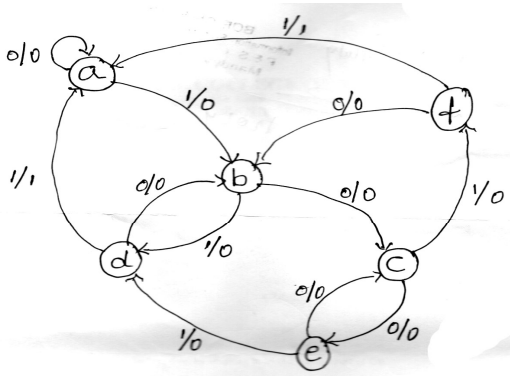


fig 5(b) 9

c. i) Analyze the mealy model asynchronous sequential circuit of Fig. 5(c) and show its stable state and corresponding outputs.

ii) Give the state diagram of the circuit as shown in Fig.5(c)

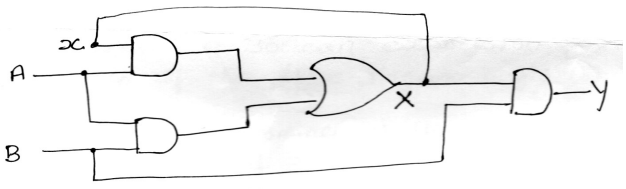


fig 5(c) 9

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