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P.E.S. College of Engineering, Mandya - 571 401
(An Autonomous Institution affiliated to VTU, Belagavi)
Third Semester, B.E. - Information Science and Engineering
Semester End Examination; Dec. - 2019
Computer Organization and Architecture

Time: 3 hrs   *Max. Marks: 100*

Note: **i) PART - A** is compulsory. **Two** marks for each question.
       ii) PART - B: Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.

Q. No.	Questions	Marks
	I : PART - A	**10**
I a.	Represent +99 in sign and magnitude and 2's complement form.	2
b.	Write the status registers of keyboard and display interface.	2
c.	List the phases used to process (execute) an instruction.	2
d.	Write the diagram of static RAM cell.	2
e.	Write the Booth's multiplier recoding table.	2
	II : PART - B	**90**
	UNIT - I	**18**
1 a.	Convert the following pairs of decimal numbers to 5-bit 2's complement numbers, and then perform addition and subtraction on each pair. Indicate whether or not overflow occurs for each case: i) 7 and 13 ii) −12 and 9.	9
b.	Explain the main functional units of a computer with neat diagram.	9
c.	A list of student marks is stored in memory. Entry for each student includes the student ID, followed by the scores in 3 tests. Write a program to find the average marks of the class scored in test 2. Assume that the processor has DIV instruction.	9
	UNIT - II	**18**
2 a.	Write a RISC style program using subroutine to add 5 numbers and store the result in memory location SUM and read parameters using register.	9
b.	Explain various shifts and rotate instruction with example used in RISC style machines.	9
c.	Define Interrupt. Explain vectored Interrupt and Interrupt nesting.	9
	UNIT - III	**18**
3 a.	Write and explain the sequence of action needed to fetch and execute the instruction Branch_if_[R3] ≠ [R7] loop.	9
b.	Explain with neat detailed timing diagram for the input transfer using synchronous bus.	9
c.	Explain the main hardware components of a processor used for execution of instruction.	9

UNIT - IV **18**

4 a. Explain the organization of 1k x 1 memory chip with the help of neat diagram. 9

b. Explain virtual memory address translation with neat schematic representation. 9

c. Explain Direct Memory Access. 9

UNIT - V **18**

5 a. Apply Booth and bit pair recoding algorithms to find the product of two 6 bit multiplicand and Multipliers where multiplicand = 110101 and multiplier = 011011. 9

b. Apply restoring division algorithm for the following numbers 43/9. 9

c. Explain Flynn's taxonomy. 9

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