***U.S.N*** | | | | | | | | | | |

# P.E.S. College of Engineering, Mandya - 571 401

***(An Autonomous Institution affiliated to VTU, Belagavi)***

## Third Semester, B.E. - Electronics and Communication Engineering

## Semester End Examination; March - 2021

## Digital Electronic Circuits

*Time: 3 hrs* *Max. Marks: 100*

***Course Outcomes***

*The Students will be able to:*

*CO1: Ability to apply the knowledge of mathematics and science to understand the operation of logic circuits and performance parameters.*

*CO2: Ability to apply the simplification techniques/methods to optimize and implement the digital functions/circuits.*

*CO3: Ability to analyze the given logic circuit based on the knowledge of digital elements.*

*CO4: Ability to design a combinational and sequential logic circuit for the given requirements/specifications.*

*CO5: Ability to understand and design the State machines with state graphs for sequential design.*

***Note:*** ***I) PART - A*** *is compulsory.* ***Two*** *marks for each question.*

***II) PART - B****: Answer any* ***Two*** *sub questions (from a, b, c) for Maximum of* ***18 marks*** *from each unit.*

| Q. No. | | Questions | Marks | BLs | COs | POs |
|---|---|---|---|---|---|---|
| | | **I : PART - A** | **10** | | | |
| I | a. | List the two bit maxterms. | 2 | L3 | CO1 | PO1 |
| | b. | Assuming ideal conditions design a *D*-flip flop using multiplexer. | 2 | L3 | CO4 | PO3 |
| | c. | Draw the schematic of a gated SR latch. | 2 | L2 | CO4 | PO3 |
| | d. | Compute the maximum number of flip-flops required to count five events. | 2 | L3 | CO5 | PO1 |
| | e. | Draw the schematic of a general Mealy machine. | 2 | L2 | CO3 | PO2 |
| | | **II : PART - B** | **90** | | | |
| | | **UNIT - I** | **18** | | | |
| 1 | a. | Simplify the expression using *K*-map;<br>i) $f(A, B, C, D) = \Sigma\, m(0, 2, 4, 6, 9, 11, 13, 15)$<br>ii) $(a,b,c,d) = a\bar{b} + cd + ac + b\bar{c}$ | 9 | L3 | CO2 | PO2 |
| | b. | Simplify the following Boolean expression using Quine-McCluskey method: $f(P, Q, R, S) = \Sigma$ m(1, 6, 8, 9, 10, 11, 14,) + $\Sigma$ d(7, 13) | 9 | L3 | CO2 | PO2 |
| | c. | Simplify the following expression using VEM technique:<br>i) $f(A, B, C, D) = \Sigma$ m(0, 2, 4, 5, 7, 9, 11, 13)<br>ii) $f(A, B, C) = \prod$ m(0, 3, 5, 6, 7) | 9 | L3 | CO2 | PO2 |
| | | **UNIT - II** | **18** | | | |
| 2 | a. | Design a combinational circuit to add 2-bit gray code number *A* and *B*. | 9 | L4 | CO4 | PO3 |
| | b. | Design and implement 2-bit binary to gray code converter, using optimum configuration multiplexers. | 9 | L4 | CO4 | PO3 |

Contd… 2

| | | | | | |
|---|---|---|---|---|---|
| c. | Illustrate the concept of combinational logic implementation using ROM and PLA. | 9 | L4 | CO4 | PO3 |
| | **UNIT - III** | **18** | | | |
| 3 a. | With required transition table and characteristic equation, analyze the operation of SR flip flop. | 9 | L2 | CO3 | PO2 |
| b. | With required timing diagram, discuss the reasons of race around condition in JK flip flop, while illustrating / highlighting the possible solutions. | 9 | L3 | CO3 | PO2 |
| c. | Convert; i) D flip flop to JK flip flop and ii) T flip flop to D flip flop | 9 | L3 | CO3 | PO2 |
| | **UNIT - IV** | **18** | | | |
| 4 a. | Design a sequential logic circuit to generate sequence 8→4→2→1 assuming appropriate initial condition. | 9 | L4 | CO4 | PO1 |
| b. | Design a sequential logic circuit to generate all the possible factors of factorial 8 (8!). | 9 | L4 | CO4 | PO1 |
| c. | Design an arithmetic circuit with two select lines $S_1$ and $S_0$ to generate the arithmetic operations as listed in Table. 4. c, draw the logic diagram. | 9 | L4 | CO4 | PO1 |

| $S_1$ | $S_0$ | $C_{in} = 0$ | $C_{in} = 1$ |
|---|---|---|---|
| 1 | 1 | $F = A$ | $F = A + 1$ |
| 0 | 0 | $F = A + B$ | $F = A + B + 1$ |
| 1 | 0 | $F = A + \overline{B}$ | $F = A + \overline{B} + 1$ |
| 0 | 1 | $F = A - 1$ | $F = A$ |

Table 4.c

| | | | | | |
|---|---|---|---|---|---|
| | **UNIT - V** | **18** | | | |
| 5 a. | For the logic diagram given in Fig. 5(a),<br>i) Write the excitation table and derive the output equations<br>ii) Write the next state equations<br>iii) Construct / write transition table<br>iv) Draw the state diagram | 9 | L4 | CO5 | PO1 |

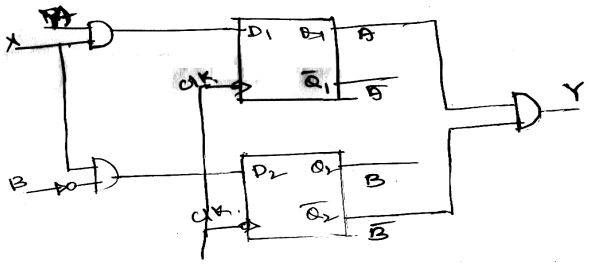


Fig. 5(a)

| | | | | | |
|---|---|---|---|---|---|
| b. | Design a logic circuit to detect the sequence 1101(Use D flip flops). | 9 | L4 | CO5 | PO1 |
| c. | Discuss the concepts of Moore and Mealy machines while accounting the instances of their suitability. | 9 | L3 | CO5 | PO1 |

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