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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fifth Semester, B.E. - Electronics and Communication Engineering
Semester End Examination; Feb. - 2021
Digital CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: To Apply the basic knowledge of Physics and mathematics to understand the MOS and derive different current equations of MOS circuits and delays of CMOS inverter circuits.

CO2: To Analyze the CMOS inverter circuit and BiCMOS circuits.

CO3: To Design combinational, sequential and Dynamic circuits based on CMOS inverters for the given specifications.

CO4: To Discuss various issues related to clocking, I/O and protection in MOS and VLSI Fabrication Process.

CO5: Work in groups to model transistors and its circuits learning new tools.

Note: ***I) PART - A*** *is compulsory.* ***Two*** *marks for each question.*
II) PART - B*: Answer any* ***Two*** *sub questions (from a, b, c) for Maximum of* ***18 marks*** *from each unit.*

Q. No.	Questions	Marks	BLs	COs	POs
	I : PART - A	**10**			
I a.	Define channel length modulation of *n*-channel MOSFET.	2	L2	CO1	PO1
b.	Define power, delay product of CMOS logic gate.	2	L2	CO1	PO1
c.	Write CMOS circuit for NOR3 gate.	2	L2	CO3	PO2
d.	Define dynamic CMOS logic circuit.	2	L2	CO3	PO2
e.	Write any two guidelines for avoiding Latch up.	2	L2	CO4	PO1
	II : PART - B	**90**			
	UNIT - I	**18**			
1 a.	Derive the expression for threshold voltage V_T interms of V_{SB} and surface potential.	9	L3	CO1	PO1
b.	Explain full scaling technique and its effect on device performance. Also calculate the drain current and power dissipation after scaling.	9	L3	CO1	PO1
c.	Calculate the threshold voltage V_{TO} at $V_{SB} = 0$ for a polysilicon gate *n*-channel MOS transistor with the following parameters: Substrate doping density $N_A = 10^{16}$ cm^{-3} Polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3} Gate oxide thickness $t_{ox} = 500\ \mathring{A}$ and oxide interface fixed charge density $N_{ox} = 4\times10^{10}\ cm^{-2},\ \eta_i = 1.45\times10^{10}\ cm^{-3}, \epsilon_{SI} = 11.7\epsilon_0, \epsilon_{ox} = 3.97\epsilon_0$.	9	L4	CO1	PO1
	UNIT - II	**18**			
2 a.	Consider a CMOS inverter circuit with the following parameters. $V_{IL} = 1.08\ V,\ V_{DD} = 3.3\ V, V_{TO,n} = 0.6\ V, V_{TO,p} = -0.7\ V, K_n = 200\ \mu A/V^2$, $K_p = 80\ \mu A/V^2$ Calculate the noise margins of the circuit. Notice that the CMOS inverters being considered here has $K_r = 2.5$ and $V_{TO,n} \neq \lvert V_{To,P} \rvert$:	9	L3	CO1	PO1

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Q.No.	Question	Marks	BL	CO	PO
b.	Analyze the oxide related capacitance of MOSFET with related equation and figure.	9	L3	CO1	PO1
c.	Discuss the calculation of interconnect delay using, i) RC delay model ii) Elmore's delay model	9	L3	CO1	PO2
	UNIT - III	**18**			
3 a.	Explain operation of CMOS transmission gates along with Bias condition and operating regions.	9	L2	CO3	PO2
b.	Design CMOS logic circuit for the function $Z = \overline{(D+E+A)(B+C)}$ and draw stick diagram using Euler's path.	9	L4	CO3	PO3
c.	Briefly discuss NOR based CMOS SR Latch circuit.	9	L3	CO3	PO3
	UNIT - IV	**18**			
4 a.	Briefly explain cascaded domino CMOS logic circuit for high performance dynamic logic circuit.	9	L3	CO3	PO3
b.	Explain the concept of voltage Bootstrapping.	9	L3	CO3	PO3
c.	Analyze the charge storage and charge leakage phenomenon at a soft node in a CMOS network.	9	L3	CO3	PO3
	UNIT - V	**18**			
5 a.	Write the figures for the process flow for the fabrication of an *nMOSFET* on *p*-type silicon.	9	L2	CO4	PO1
b.	Briefly explain BiCMOS inverter circuit with resistive base pull down.	9	L3	CO2	PO2
c.	Analyze the on-chip clock generation using ring oscillator also clock distribution using H-tree and three-level buffered network.	9	L3	CO4	PO1

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