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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fifth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Feb. - 2021

DSP Processor and Applications

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: Distinguish between the DSP Processor and general purpose processor.

CO2: Analyze the architecture features of Digital signal processor using basic digital circuit knowledge.

CO3: Develop programs for digital filters using DSP processor for various situations and demonstrate utility of DSP processor in various signal processing applications.

CO4: Apply the logical and signal processing concepts to develop algorithms for DSP processor.

CO5: Design the interface to connect specified memory and signal converters.

***Note**: I) **PART - A** is compulsory. **Two** marks for each question.*

*II) **PART - B**: Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.*

Q. No.	Questions	Marks	BLs	COs	POs
	I: PART - A	**10**			
1 a.	If a sum of 256 products is to be computed using a pipelined MAC unit, and if the MAC execution time of the unit is 100 nsec, what will be the total time required to complete the operation?	2	L3	CO4	PO1
b.	Describe the operation of the following *MPY* instructions: i) *MPY 13, B* ii) *MPY #01234, B*	2	L4	CO3	PO4
c.	What values are represented by the 16 bit fixed point number *N* = 4000h in the *Q15* and *Q17* notations?	2	L3	CO4	PO1
d.	Determine the timing parameters for a 16-bit data communication in a DSK configured for a clock divisor of 6. The oscillator clock is at 12.288 MHz.	2	L4	CO4	PO1
e.	Draw the block diagram of a DSP system.	2	L2	CO1	PO1
	II: PART - B	**90**			
	UNIT -I	**18**			
1 a.	Explain circular and bit reversed addressing modes.	9	L3	CO4	PO1
b.	With neat diagram, explain accumulator guard bits and saturation logic.	9	L2	CO2	PO2
c.	List all the basic feature for implementing; $y(n)=\sum_{i=0}^{N-1} h(i)\,x(n-i) \quad n=0,1,2.....$ in the DSP architecture.	9	L3	CO2	PO2
	UNIT - II	**18**			
2 a.	With neat block diagram, explain barall shifter of the TMS320C54XX processor.	9	L2	CO2	PO2

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	b. With neat diagram, explain the circular addressing mode for TMS320C54XX processor.	9	L2	CO2	PO2
	c. Draw the memory map for TMS320C54XX processor and explain processor bits for configuring the on chip memories.	9	L3	CO2	PO2
	UNIT - III	**18**			
3 a.	Explain how the FIR filter algorithm can be implemented using TMS320C54XX processor?	9	L4	CO4	PO1
	b. What is PID controller? Explain its operation. With neat diagram, explain PID control implementation.	9	L4	CO4	PO1
	c. Draw the signal flow graph of 2-point, 4-point and 8-point DFT. And also explain general butterfly computation structure.	9	L2	CO2	PO2
	UNIT - IV	**18**			
4 a.	With a neat diagram, explain the CODEC interface unit.	9	L5	CO5	PO3
	b. Draw and explain flowchart of interrupt handling by the processor.	9	L5	CO5	PO3
	c. Design a data memory system with address range 000800h-000FFFh for a C5416 processor use 2k×8 SRAM memory chip.	9	L5	CO5	PO3
	UNIT - V	**18**			
5 a.	Draw and explain a DSP based biotelemetry receiver implementation.	9	L4	CO3	PO4
	b. With neat diagram, explain a schematic diagram of the human vocal apparatus.	9	L4	CO3	PO4
	c. Draw the block diagram for hard disk drive servo control system. Explain it in detail.	9	L4	CO3	PO4

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