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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fifth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Feb. - 2021

System Verilog (Technical Skills - I)

Time: 2 hr. *Max. Marks: 50*

Course Outcomes

The Students will be able to:

CO1: Understand the system verilog language constructs.

CO2: Understand the system verilog OOPs facilities and framework for the verification.

CO3: Develop programs by applying the system verilog facilities and framework.

CO4: Explore and understand modern software tools to perform different operations in system verilog.

CO5: Develop the capability to learn on your own individually and in group to explore advanced technologies in system verilog.

***Note: All** questions are **compulsory** and each question carries **TWO** marks.*

Q. No.	Questions	BLs	COs	POs
1.	A net type of wire labeled A is connected to a net type of tri labeled B, assuming both of same width the assignment will lead to a) Compilation error b) Warning c) No warning no errors d) Depends on the tool	L3	CO1	
2.	If two signals simultaneously tries to drive an element declared as wire than it results in a) Compilation error b) Warning c) Value resolved on the basis of driver logic is assigned to the element d) Either the first or the last signal value is assigned to the element	L3	CO1	
3.	Aggregate operations like copy and compare are applicable to a) Fixed arrays b) Dynamic arrays c) Associate and fixed arrays d) Associate and dynamic arrays e) Dynamic and fixed arrays	L2	CO1	
4.	The value of x and z in the following context will be enum {x, y = 3, z} state; a) x = 2, z = 4 b) x = 1, z = 4 c) x = 0, z = 4 d) x = 0, z = 3	L4	CO1	
5.	The strings in System verilog ends with a) Newline character b) Null "\0" character c) Last character of the string d) Space as special character	L2	CO1	
6.	A variable or a signal defined through the typedef in Systemverilog is resolved during a) Simulation b) Compilation c) Simulation and Synthesis d) Compilation and Synthesis	L4	CO2	

Contd… 2

7. The difference between function and task is
   a) Function supports sequential execution and task doesn't
   b) Function doesn't support delay and task does — L2 CO2
   c) Function must return a value and task will not
   d) Both b and c

8. Which of the following statement is true
   a) Function can be turned into a task
   b) Task can be turned into a function — L2 CO2
   c) Function and task are not interchangeable
   d) Interchange ability of function and task Depends on the way of their implementation

9. Which of the following statement is true
   a) Function can call a task b) A task can call a function — L2 CO2
   c) Function cannot call task d) A task cannot call function e) b and c

10. The value returned by the function sum is

```
x = sum(10,5);
function int sum(input inta,b);
int d;
  sum = a+b;
  d = a + sum;
endfunction
```

   — L4 CO2

   a) 25 b) 10 c) 15 d) 0

11. A local variable in system verilog is initialized
   a) During simulation b) Before the start of simulation — L5 CO3
   c) At the start of simulation d) Depending on coding style

12. When a handle is declared
   a) It is initialized with specific location address b) It is initialized to null — L4 CO3
   c) Memory is allocated d) Memory is not allocated
   e) a and d f) b and d

13. By default new() method initializes class variables to — L2 CO3
   a) 0 b) X c) 0 or X d) Z

14. Deep copy implies
   a) Handles will be copied
   b) Objects will be copied — L3 CO3
   c) Handles will not be copied
   d) a and b
   e) b and c

Contd… 3

15. Randomization is required in system verilog

a) As it is not possible to write direct test cases

b) As it is not possible to write all the possible direct test cases

c) As requirements can be random L2 CO3

d) As requirements can be vast

e) a and c

f) b and d

16. execution of the following code will display _____

```
class packet;
  rand byte addr;
  rand byte data;
endclass
module rand_methods;
  initial begin
    packet pkt;
pkt = new();
pkt.addr.rand_mode(0);
pkt.randomize();
    $display("\taddr = %0d \t data = %0d",pkt.addr,pkt.data);
    end
endmodule
```

L5 CO4

a) addr = 0 and data = 0 b) addr = 10 and data = 0

c) addr = 0 and data = 70 d) addr = 10 and data = 70

17. Which of the following statement is syntactically incorrect?

a) randc rand bit [2:0] addr2; b) randcbit [2:0] addr2; L4 CO4

c) rand bit [2:0] addr2; d) randc bit [0:2] addr2;

18. Assertions are

a) Pieces of declarative code that cannot be simulated

b) Pieces of declarative code that can be simulated

c) Code to check relation between signals in a design L2 CO4

d) a and c

e) b and c

19. A class can contain

a) Single cover group

b) Multiple cover groups L2 CO4

c) Single or multiple cover groups

d) No cover group

Contd… 4

20. Random device configuration helps

    a) To test the design for all the possible modes

    b) To test the design for as many modes as possible — L3 CO4

    c) To test the design for critical modes

    d) To test the design for specific modes

21. In system verilog , the default mail box size is

    a) 100 messages

    b) Undefined — L3 CO5

    c) Depends on tool

    d) Zero

22. In system verilog, an event

    a) Synchronizes threads

    b) Controls semaphores — L2 CO5

    c) Controls message flow

    d) a, b and c

    e) b and c

23. Semaphore is used to control

    a) Bus access

    b) Bus transaction rate — L3 CO5

    c) Bus access and bus transaction rate

    d) Bus access such that only one driver can access the bus at any given time

24. In system verilog, an event

    a) Static

    b) Dynamic — L3 CO5

    c) Can be passed to Queues and functions.

    d) a and c

    e) b and c

25. Coverage is

    a) Number of bins*Number of sampled values

    b) Number of bins/Number of Sampled Values — L4 CO5

    c) Number of Sampled Values/Number of bins

    d) Number of bins + Number of sampled values

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