U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Electrical and Electronics Engineering

Semester End Examination; March - 2021

Digital Electronics Circuits

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: To analyze the different switching algebra theorems and apply them for logic functions.

CO2: Explain and analyze the Karnaugh map for a few variables & combinational circuits: half adders / subtractors, encoders / decoders.

CO3: Explain and analyze the bistable element and the different latches and flip flops.

CO4: Explain and analyze sequential circuits, like counters and shift registers.

CO5: Explain and analyze the concepts of A/D and D/A converters.

Note: ***I) PART - A*** *is compulsory.* ***Two*** *marks for each question.*

II) PART - B*: Answer any* ***Two*** *sub questions (from a, b, c) for Maximum of* ***18 marks*** *from each unit.*

Q. No.	Questions	Marks	BLs	COs	POs
	I : PART - A	**10**			
I a.	What is the difference between latch and flip flop?	2			
b.	State the DeMorgan theorem.	2			
c.	Write difference between Multiplexer and Demultiplexer.	2			
d.	Write the diagram for flash type ADC.	2			
e.	What is a Counter? Mention different types of Counters.	2			
	II : PART - B	**90**			
	UNIT - I	**18**			
1 a.	i) Convert the given expression in standard SOP from; $f(A, B, C) = AC+AB+BC$ ii) Convert the given expression in standard POS form; $Y = A.(A+B+C)$	9			
b.	Expand $f_1 = a + ab + a\bar{c}d$ into minterms and $f_2 = a(b+c)(a+c+\bar{d})$ into maxterms.	9			
c.	Staircase light is controlled by two switches; one is at the top of the stairs and other at the bottom of the stair. i) Write the truth table for the system ii) Write the logic equations in SOP form iii) Realize the circuit using basic gates iv) Realize the circuit using minimum number of NAND gates	9			
	UNIT - II	**18**			
2 a.	Minimize the expression using Quine Mccluskey method; $Y = \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}\bar{D} + AB\bar{C}D + A\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D}$	9			

Contd… 2

b. Write the *k*-map for the Boolean function and minimize the expression; 9

i) $f(w, x, y, z) = \Sigma m(2, 9, 10, 11, 13, 14, 15) + d(3, 4, 5)$

ii) $F(A, B, C, D) = \prod M(1, 2, 3, 5, 9, 10, 12, 13)$

c. Explain the implementation of full adder with block diagram and truth table. 9

UNIT - III **18**

3 a. Explain 4-bit priority encoder with truth table and *k*-map simplification also implement using logic diagram. 9

b. Construct full subtractor using Demultiplexer (1:8) with truth table and implementation. 9

c. Compare;

i) Combinational and Sequential logic circuit 9

ii) Synchronous and Asynchronous sequential circuit

UNIT - IV **18**

4 a. Explain Moore model and Mealy model using JK flip flop. 9

b. A sequential circuit with 2 D flip flops *A* and *B* and input *X* and output *Y* is specified by the following next state and output equation:

$A(t+1) = AX + BX \qquad B(t+1) = A'X \qquad Y = (A+B)X'$ 9

i) Draw the logic diagram of the circuit

ii) Derive the state table

iii) Derive the state diagram

c. Explain 3-bit synchronous binary counter with timing diagram and state sequence. 9

UNIT - V **18**

5 a. Explain ramp type DAC with neat block diagram for voltage to time conversion. 9

b. With the help of a neat diagram, explain the working of R-2R ladder network. 9

c. What are different parameters on which A/D and D/A conversion techniques are based? 9

* * *