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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec. - 2019

Analog Electronic Circuits

Time: 3 hrs *Max. Marks: 100*

Note: I) **PART - A** is compulsory. **Two** marks for each question.
II) **PART - B**: Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.

Q. No.	Questions	Marks
	I : PART - A	**10**
I a.	Define slew rate.	2
b.	Draw the circuit diagram of op-amp differentiating circuit.	2
c.	A square wave generator using 555 has V_{CC} = 10 V, R_1 = 10 kΩ, R_2 = 5 kΩ and C_1 = 0.01 μf. Determine the circuit output frequency.	2
d.	State Barkhausen criteria for sustained oscillation.	2
e.	Draw the block diagram of PLL system.	2
	II : PART - B	**90**
	UNIT - I	**18**
1 a.	Sketch the diagram of Direct-coupled inverting amplifier. Design an inverting amplifier using 741 Op-amp. The voltage gain is to be 50 and the output voltage amplitude is to be 2.5 V. I_{Bmax} of 741 is 500 μA.	9
b.	Draw the circuit diagram of difference amplifier. Derive an expression for V_O for a difference amplifier.	9
c.	Illustrate how input impedance can be increased in capacitor coupled voltage follower.	9
	UNIT - II	**18**
2 a.	Design the voltage source in Fig. Q2(a) to provide an output of 9 V to a 500 Ω load. The available supply is ±12 V and the potentiometer is to be included to adjust for approximately ± 10% tolerance on the Zener diode voltage.	9

Data : IN749 V_Z = 4.3V.

$I_{B(max)}$ = 500mA

I_Z = 20mA

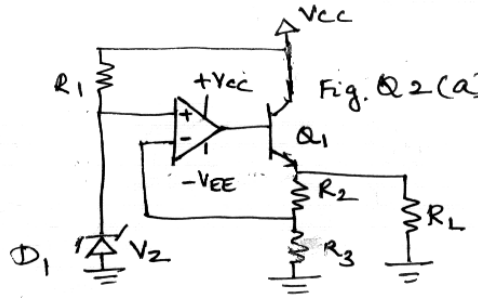

Fig. Q2(a)

b.	With neat diagram, explain the working of voltage level detector when i) $V_{R3} \geq V_z$ ii) $V_{R3} \leq V_z$	9

Contd...2

c. Design an Op-amp differentiating circuit to produce a 5 V output when the input changes by 1V in 100 μs. Use Bipolar Op-amp. Draw the circuit diagram. 9

UNIT - III **18**

3 a. With neat diagram, explain the working of non saturating precision half wave rectifier. 9

b. With neat diagram, explain the working of sample and hold circuit. 9

c. Design a 555 astable multi-vibrator to give a 2 kHz pulse repetition frequency with a 70% duty cycle. Use V_{CC} = 18 V, I_{th} = 0.25 mA, I_{trig} = 0.5 μA. Draw the diagram. 9

UNIT - IV **18**

4 a. With neat diagram, illustrate how combination of integrator and Schmitt trigger can be used to produce triangular and rectangular waveform. 9

b. Design a phase shift oscillator to produce a 3 kHz output frequency. The Op-amp is to use ±12 V supply. $I_{B(max)}$ for 741 Op-amp is 500 μA. Use 741 Op-amp. 9

c. Design a voltage regulator in Fig. Q4(c) to produce a 12 V output with a 50 mA load current. Use IN757 Zener diode with V_z = 9.1V. Use Op-amp 741. 9

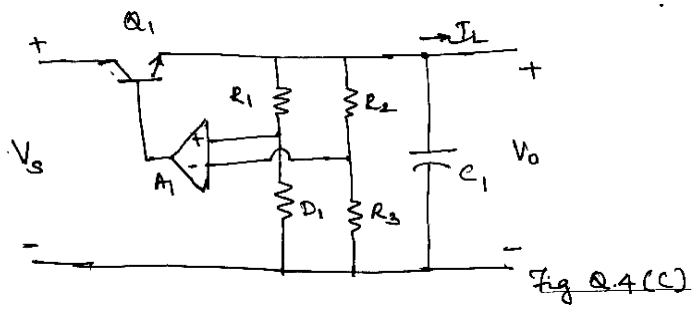

Fig Q.4(c)

UNIT - V **18**

5 a. With neat diagram, explain the working of 3-bit R-2R DAC. 9

b. With neat diagram, explain the working of digital RAMP ADC. 9

c. Determine the average level of the phase detector output wave in Fig. Q5(c) If the phase difference is 2.3 radians, the waveform frequencies are 10 kHz and the pulse amplitude is ±5 V. Calculate the phase detector sensitivity. 9

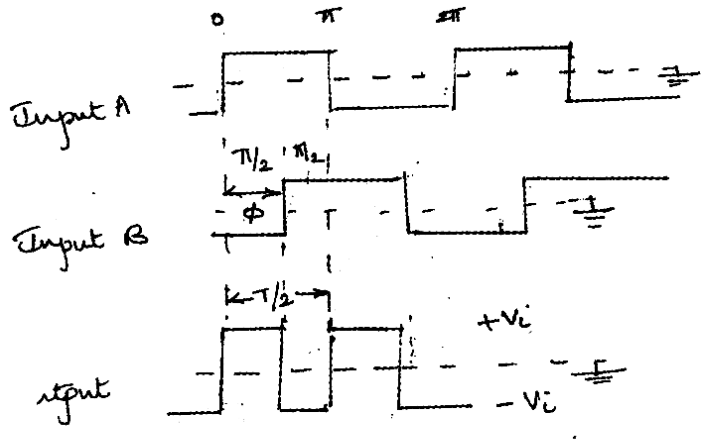

Fig 5(c)

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