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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec. - 2019

Digital Electronic Circuits

Time: 3 hrs *Max. Marks: 100*

Note: i) PART - A is compulsory. **Two** marks for each question.
ii) PART - B: Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.

Q. No.	Questions	Marks
	I : PART - A	**10**
I a.	Define canonical minterm and canonical maxterm.	2
b.	What are the differences between synchronous and asynchronous counters?	2
c.	Draw the schematic of full adder using two half adders.	2
d.	What is race around condition in JK flip-flop? When does it occur?	2
e.	Compare Moore and Mealy models.	2
	II : PART - B	**90**
	UNIT - I	**18**
1 a.	Simplify the following Boolean expressions using k-map: i) $f(ABCD) = \overline{A}\overline{B}C + AD + B\overline{D} + C\overline{D} + A\overline{C}$ ii) $F(wxyz) = (w + x + \overline{y}).(\overline{x} + \overline{z}).(\overline{w} + y).(x + y)$	9
b.	Find the minimal sum of the Boolean expression using Quine-McCluskey method, $f = \sum m(1, 3, 6, 8, 9, 10, 12, 14) + \sum d(7, 13)$	9
c.	Simplify the following expressions using VEM technique: i) $f(ABCD) = \sum m(2, 3, 5, 6, 8, 11, 12, 13)$ ii) $Y = \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}CD\overline{E} + \overline{A}B\overline{C}\overline{D}E + \overline{A}BCD + ABC\overline{D} + A\overline{B}C\overline{D}F + \overline{A}BC\overline{D}\overline{F} + ABCDE$	9
	UNIT - II	**18**
2 a.	i) Implement Full subtractor using a suitable decoder. ii) Design a 2 bit comparator and implement using basic gates.	9
b.	Implement $f = ad + b\overline{c} + bd$ using (i) 16:1 MUX (ii) 8:1 MUX (iii) 4:1 MUX	9
c.	Write a short note Read Only Memory (ROM) and Programmable Logic Array (PLA).	9

Contd...2

UNIT - III **18**

3 a. Derive the characteristic equations of SR Flip flop and JK Flip flop. 9

b. Explain the operation of Master-Slave JK flip flop using the logic diagram, truth table and clock diagram. 9

c. Convert; (i) SR Flip flop to JK Flip flop (ii) JK flip flop to D flip flop 9

UNIT - IV **18**

4 a. Explain with suitable logic diagram and truth table the operation of the following shift registers: 9

(i) Serial-in-Serial-out (ii) Serial-in-Parallel-out

(iii) Parallel-in-Serial-out (iv) Parallel-in-Parallel out

b. Design a counter using JK flip flop to count the following sequence 9

$0 \rightarrow 1 \rightarrow 3 \rightarrow 7 \rightarrow 6 \rightarrow 4 \rightarrow 0$

c. Design an arithmetic circuit with two select lines S_1 and S_0 that generates the following arithmetic operations. Draw the logic diagram. 9

S_1	S_0	Cin = 0	Cin = 1
0	0	F = A	F = A + 1
0	1	F = A + B	F = A + B + 1
1	0	$F = A + \overline{B}$	$F = A + \overline{B} + 1$
1	1	F = A – 1	F = A

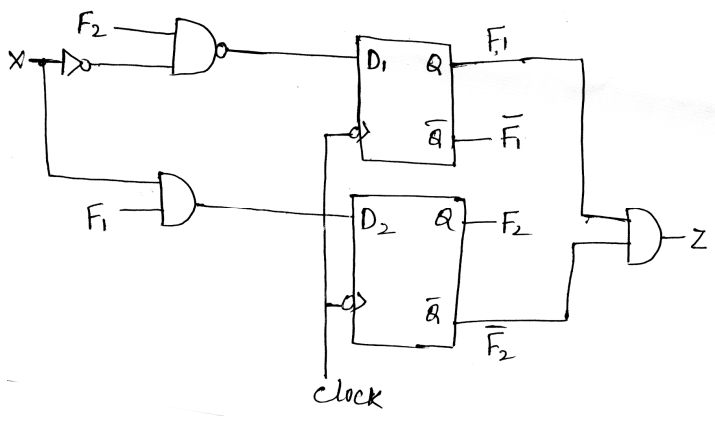
UNIT - V **18**

5 a. For the logic diagram given below: 9

i) Write the excitation table and derive the output equations

ii) Write the next state equations

iii) Construct a transition table iv) Draw the state diagram



b. Design a Mealy type sequence detector to detect a serial input 101 (use D F/F). 9

c. Differentiate Mealy state machine and Moore State machine. 9

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