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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Electricals and Electronics Engineering

Semester End Examination; Dec.-2019

Digital Electronics Circuit

Time: 3 hrs *Max. Marks: 100*

Note: i) PART - A is compulsory. **Two** marks for each question.

ii) PART - B: Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.

Q. No.	Questions	Marks
	I : PART - A	**10**
I a.	Use 2's complement method to perform M – N where, M and N are binary numbers given by M = 1010100, N = 1000100.	2
b.	Given $f(a,b,c)=\bar{b}+a\bar{c}$, Write $f=\pi m(\quad\quad)$	2
c.	Obtain the characteristic equation of JKFF.	2
d.	Number of Flip flops required to build a binary counter that counts from 0 to 13 is _____	2
e.	Define Fan-in and Fan-out as applied to logic families.	2
	II : PART - B	**90**
	UNIT - I	**18**
1 a.	Represent the following in both Canonical minterm and Canonical maxterm forms in decimal notation, i) $f=\bar{x}y+yz$ ii) $f=(\bar{a}+b)(b+\bar{c})$	9
b.	Convert the given expression in standard POS form: i) $f(A,B,C)=(A+B)(B+\overline{C})(A+C)$ ii) $f(A,B,C)=A.(A+B+C)$	9
c.	Find the complement of the following functions: $f_1=\bar{x}y\bar{z}+\bar{x}\bar{y}z$ $f_2=x(\bar{y}\,\bar{z}+yz)$	9
	UNIT - II	**18**
2 a.	Obtain the simplified expression in POS form, i) $f(a,b,c,d)=\bar{a}\bar{b}d+bcd+a\bar{b}d+b\bar{c}\bar{d}$ ii) $f(a,b,c,d)=\sum m(1,3,5,7,8,10,12,13,14)+\sum d(4,6,15)$	9
b.	Obtain a minimal sum for the Boolean function *f(a, b, c, d)* = ∑m(0, 2, 3, 4, 8, 10, 12, 13, 14) using Quine-McCluskey method.	9
c.	Explain the working of carry look ahead adder with relevant circuit diagrams.	9

Contd…2

UNIT - III **18**

3 a. Implement a full adder using a 2:4 decoder. 9

b. Realize the function f (a, b, c) = $\sum$ m(1,4,5,7) using 4:1 Mux using b and c as the select lines. 9

c. i) Convert SR flip-flop to JK flip-flop
ii) Convert D flip-flop to T flip-flop 9

UNIT - IV **18**

4 a. With a neat block diagram, bring out the differences between Mealy and Moore Models. 9

b. With a neat diagram, explain the working of a SISO, PIPO – 4 bit shift register. 9

c. Design a synchronous Mod 6 counter for the sequence 0, 2, 3, 6, 5, 1, 0….. using D flip-flops. 9

UNIT - V **18**

5 a. With the help of a neat diagram, explain the Binary weighted resister D/A converter. 9

b. With the help of a neat diagram, explain the working of flash ADC. 9

c. With a neat diagram the operation of a two input TTL NAND gate. 9

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