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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Information Science and Engineering

Semester End Examination; Dec. - 2019

Digital Design

Time: 3 hrs *Max. Marks: 100*

Note: I) **PART - A** is compulsory. **Two** marks for each question.
II) **PART - B**: Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.

Q. No.	Questions	Marks
	I : PART - A	**10**
I a.	What is the Boolean function obtained for the following truth table:	2

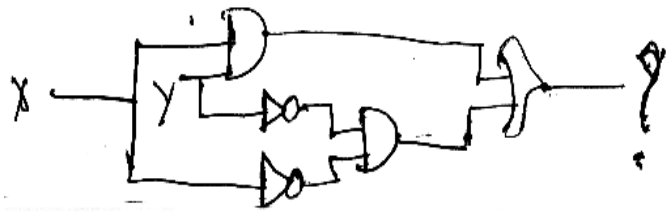
x	y	$f(x, y)$
0	0	0
0	1	0
1	0	1
1	1	1

b. Obtain the minimal form from the K-map — 2

a \ bc				
	1	X	X	1
			1	X

c. Give the excitation table of JK flip flop. — 2

d. What does the following gate gives the output? — 2



e. What is the number of flip flops required to design mod-200 counter — 2

	II : PART - B	**90**
	UNIT - I	**18**
1 a.	Express –19, 750 is 2's complement representation. Then show how this number is stored at address 2000. Use hexadecimal notation to compression the data.	9
b.	Design a combinational circuit whose output is 1 for the binary number > 5 and <10 and numbers from 10 - 15 are don't care condition.	9
c.	Define universal gates. Implement the following function: i) Nand gates only ii) Nor gates only iii) Nor gates only $g = x\acute{y} + xy + xy\acute{}$	9

Contd…2

UNIT - II **18**

2 a. Simplify the given SOP expression using Quine McCluskey method: 9

$F(a, b, c, d) = \sum m(2, 3, 10, 11, 12, 13, 14,15) + d(0, 1)$

b. Realize the following expression using decoder: 9

i) $f = xy + x'y + xy'$ ii) $f = xyz + x'z + xy$ iii) $f = x'z + x'y + z'$

c. Implement the following using PLA 9

$f(A, B, C)=\sum m(0, 2, 4, 5, 6)$

$f(A, B, C) = \sum m(0, 1, 3, 5)$

UNIT - III **18**

3 a. Discuss half subtractor and Full subtractor with a neat logic circuit. 9

b. Discuss the operation of JK flip flop with truth table and design the JK flip flop circuit using only Nand gates. 9

c. Convert the following: 9

i) RS flip flop to JK flip flop ii) JK flip flop to T flip flop

UNIT - IV **18**

4 a. Explain the operation of 4-bit serial in serial out shift register with neat circuit diagram for 4-bit data 1011. 9

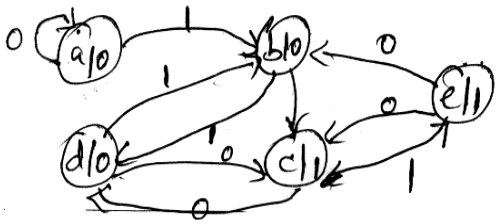
b. Design a mod-6 counter using decade CD user and also explain the circuit diagram and truth table of decade counter. 9

c. Determine the number of possible states in a counter composed of the following number of flip flops: i) 8 ii) 7 iii) 9 9

UNIT - V **18**

5 a. Differentiate between Moore Model and Mealy model with appropriate state transition diagrams. 9

b. Reduce state transition diagram using row elimination method and Implication Table method.



9

c. How can essential Hazard to be prevented in asynchronous sequential circuits. 9

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