U.S.N					



P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)
hird Samester, B.F., Information Science and Engineer

Third Semester, B.E. - Information Science and Engineering Semester End Examination; Dec. - 2019

Computer Organization and Architecture

Time: 3 hrs Max. Marks: 100

Note: i) PART - A is compulsory. Two marks for each question.

ii) PART - B: Answer any <u>Two</u> sub questions (from a, b, c) for Maximum of 18 marks from each unit.

Q. No.	Questions	Marks					
C	I : PART - A	10					
I a.	Define pipelining and what is the use of addressing mode?	2					
т а. b.	What is bus arbitration? Give the expansion of INTA.						
c.	-						
С.	Name the two techniques used to generate control signals for execution of instructions in a computer.						
d.	Name the two types of cache memories.						
e.	. What is the maximum number of summands that are required to multiply two n -bit numbers in						
	case of fast multiplication method?						
	II : PART - B	90					
	UNIT - I	18					
1 a.	Explain the functional units of computer with diagram.	9					
b.	Consider the memory system of a computer storing the following data:						
	Address Data						
	4000 00111000						
	4001 00110100						
	4002 00110010						
	4003 00111001	9					
	Interpret the storage as numbers in the manner indicated below and find their decimal values in						
	each case;						
	i) Big endian storage of 2 Hex words of 4 digits each						
	ii) Big endian storage of 2 BCD words of 4 digits each						
	iii) Little endian storage in ASCII, of a 4 digit signed Hex word						
c.	Give the significance of an addressing mode. Also discuss any four addressing modes.	9					
	UNIT - II	18					
2.	Write an Assembly program using index addressing mode to add list of numbers stored in the						
	memory locations Num1, Num2,, Numn. The total number of numbers in the list is	9					

present in the memory location N. Store the result in memory location SUM.

P18	IS35 Page No	. 2
b.	Write the code to implement Safe Push and Safe Pop operations on stack.	9
c.	With neat diagrams, explain distributed bus arbitration technique.	9
	UNIT - III	18
3 a.	Write the control sequence for executing the following instruction using single bus	
	organization:	9
	Sub R1, –(R2)	
b.	With a neat diagram, explain how control signals are generated using micro programmed control?	9
c.	With a neat diagram, explain how control signals are generated using hardwired control?	9
	UNIT - IV	18
4 a.	Describe the operation of 2M x 8 asynchronous DRAM chip.	9
b.	Explain memory hierarchy in a computer based on speed, cost and size with neat representation.	9
c.	Explain the read / write operation of an SRAM cell designed using CMOS, with the help of neat diagram.	9
	UNIT - V	18
5 a.	Multiply the following pairs of numbers using fast multiplication method:	
	i) +13 X -6	9
	ii) +09 X +15	
b.	With an algorithm, compute 8/3 using restoring division method.	9
c.	Compare single-core, multi-processor and multi-core architectures.	9