Space Vector Pulse Width Modulation for DC-AC converter

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***Abstract*—This paper deals about the concept of space vector pulse width modulation for DC-AC converter. Converter used here is nothing but a three phase inverter. Six pulses are generated for triggering switching devices used in the inverter. Based on these pulses inverter is delivering its three phase output voltage in the load terminals. Star connected resistive and capacitive load is used here in the inverter output. Two sinusoidal signals are used as input for this svpwm unit. Svpwm technique is one of the most recent trends in the pulse generation. Compared to conventional pwm and sinusoidal pwm this svpwm generates the precise pulses which is required for the three phase inverters. This svpwm generates the pulses based on the sector formation. Moreover output voltage of this inverter is formed with the reduced value total harmonic distortion.**

Index Terms - ***Sector,Alpha beta,SVPWM,RC,THD***

I. INTRODUCTION

Three phase inverters are mostly used in all industries. So this inverter must be properly operated by giving pulses. This pulse generation can be made by several ways namely sinusoidal PWM, multiple PWM, and SVPWM etc. But the most efficient way of generating pulse is space vector pulse width modulation (SVPWM). Now days this method is utilized by most of the designers because of its merits compared to other pulse generation schemes. Therefore in this paper, svpwm principle of operation is explained and modeling of the svpwm is also done. In this svpwm model, alpha, beta is used as a source. Moreover load used in this model is RC load.

II. PRINCIPLE OF OPERATION OF SVPWM

Consider the star connected RC load, the reference voltage vector for this will be,

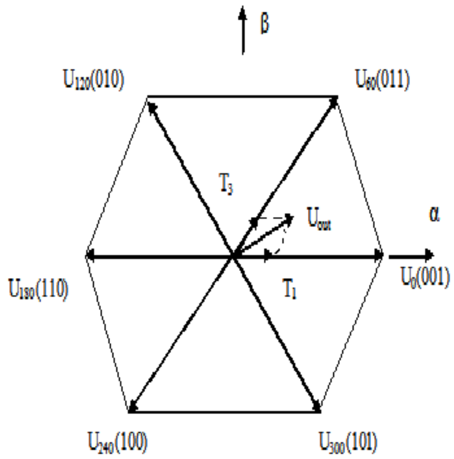
$$V_{out}=2(V_{an}+V_{bn}e^{j2\pi/3}+V_{cn}e^{j4\pi/3})/3 \quad (1)$$

Where V_{an}, V_{bn}, V_{cn} are motor phase voltages

V_{out} in any switching period can be calculated based on voltage vector compound and voltage second balance principle. The calculated V_{out} is,

$$V_{out}=T_kU_{sk}/T+T_{K+1}U_{SK+1}/T+T_0U_{000}/T+T_7U_{111}/T \quad (2)$$

Where T is switching period and equal to carrier wave period. T_k, T_{K+1} are operating time of U_{SK}, U_{SK+1} respectively. T0, T7 are operating time of U000,U111 respectively.



Fig(a)voltage space vector of three phase voltage type inverter.

In this fig(a) ,the first section can be expressed as,

$$V_{out}=T_1U0/T+T_3U_{60}/T \quad (3)$$

$$T= T_1+T_3+T_0 \quad (4)$$

The voltage vector alpha-beta can be expressed as,

$$V_\alpha= T_1U0/T+T_3U_{60}Cos(\pi/3)/T0 \quad (5)$$

$$V_\beta= T_3U60Sin(\pi/3)/T \quad (6)$$

If U0=U60 then 2Vdc/3 then equations (5) and (6) becomes,

$$T1=3TV_\alpha/2V_{dc}-\sqrt{3}TV_{beta}/2V_{dc} \quad (7)$$

$$T_3=3TV_{beta}/V_{dc} \quad (8)$$

$$T_0=T-T_1- T_3 \quad (9)$$

If $T_2=T_3$, T_{aon}, T_{bon} and T_{con} can be calculated for the upper bridge of the inverter as follows.

$$T_{aon}=(T-T_1-T_2)/4 \quad (10)$$

$$T_{bon}= T_{aon}+ T_1/2 \quad (11)$$

$$T_{con}= T_{bon}+ T_2/2 \quad (12)$$

By knowing the above values, it is easy to operate the bridge which is used in the three phase inverter.

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TABLE FOR SPACE VECTOR PULSE WIDTH MODULATION

Space vector		Switching state(Three phases)	ON state switch	Vector definition
Zero vector	V_0	[1 1 1]	S_1,S_3,S_5	0
	V_7	[0 0 0]	S_4,S_6,S_2	
Active vector	V_1	[0 0 1]	S_4,S_6,S_5	$V_1=(2/3)V_de^{j0}$
	V_2	[0 1 1]	S_4,S_3,S_5	$V_2=(2/3)V_de^{j60}$
	V_3	[0 1 0]	S_4,S_3,S_2	$V_3=(2/3)V_de^{j120}$
	V_4	[1 1 0]	S_1,S_3,S_2	$V_4=(2/3)V_de^{j180}$
	V_5	[1 0 0]	S_1,S_6,S_2	$V_5=(2/3)V_de^{j240}$
	V_6	[1 0 1]	S_1,S_6,S_5	$V_6=(2/3)V_de^{j300}$

Table 1: Switching states of SVPWM

Some assumptions are made between the above table vectors and voltage vectors which are available in fig (a).
The assumptions are,

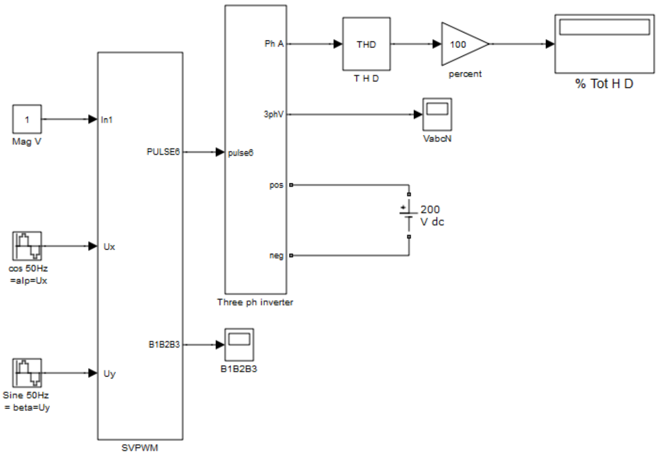
$$V_1=U_0$$
$$V_2=U_{60}$$
$$V_3=U_{120}$$
$$V_4=U_{180}$$
$$V_5=U_{240}$$
$$V_6=U_{300}$$

In this table 1, all switching states are explained clearly. According to these switching states, there are eight vectors. V_0 is the zeroth vector and V_7 is the seventh vector. From these two individual vectors, voltages are formed with the value of "0".This two vectors are also known as null vectors or zero vectors. By using the rest of the vectors, it is easy to get voltage values. V_1, V2, V3, V4, V5, V6 are the active vectors. In order to get V_1 vector, angle of banking under consideration is "0".This will give the vector value of $V_1= (2/3)V_de^{j0}$. In order to get V_2 vector, angle of banking under consideration is "60".

This will give the vector value of $V_2= (2/3)V_de^{j60}$.Similarly, to get V_3 vector, angle of banking under consideration is "120".This will give the vector value of $V_3= (2/3)V_de^{j120}$.To get V_4 vector, angle of banking under consideration is "180".This will give the vector value of $V_4= (2/3)V_de^{j180}$.To get V_5 vector, angle of banking under consideration is "240".This will give the vector value of $V_5= (2/3)V_de^{j240}$. To get V_6 vector, angle of banking under consideration is "300". This will give the vector value of $V_6=(2/3)V_de^{j300}$.

III. SIMULATION OF THE SVPWM

Simulation of the svpwm is carried out in matlab software. This simulation diagram consists of several blocks. Each and every block has its subsystem. All individual blocks are put together will deliver the required three phase ac voltage.



fig(b) simulation model of the SVPWM.

Simulation model of the svpwm is shown in fig(b).Ac signal with 50 Hz is given as alpha with 90 degree phase shift. Ac signal with 50 Hz is given as beta with 0 degree phase shift. By using this alpha, beta signals B_1, B2, B3 signals are formulated.U_x and U_y also taken out from this unit. This is nothing but alpha beta signals. Then these B_1, B2, B3 signals are fed to the sector formation unit. Based on this B_1, B2, B3 signals each and every sector is formed. After formation of the sectors, it is necessary to form the pulses. These pulses are required pulses for the three phase inverter. This inverter is fed with 200V dc supply. Then output of this inverter is taken out from the output terminals for supplying loads as well as for measurements. Total harmonic distortion of this inverter output will be very low. The overall svpwm operation can be identified by knowing the following:

(a).Sector formation block:

Sector formation block is there in svpwm block which is shown in fig (b).B_1, B2, B3 signals are given as input to the relational operator. Then the relational operator output is given to the logic gates to form the various sectors. These sectors are namely sector1 (001), sector2 (011), sector3 (010), sector4 (110), sector5 (100) and sector6 (101). These sectors are going to be used in the pulse generation unit. AND gates and NOT gates are used mainly to form these sectors. Three input AND gates are used to form the various sectors. Each and every AND gate is connected with minimum one NOT gate. This sector formation block is inbuilt in the svpwm block. This block plays a vital role in generation of the pulses. This block is one of the supporting block in the svpwm unit.

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(b).PWM signal generation block by sawtooth reference waveform:

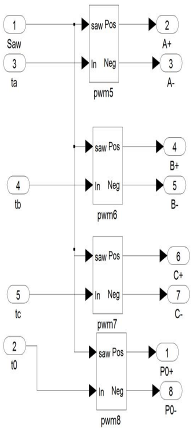


Fig (c) PWM signal generation block.

PWM signal generation block is shown in Fig (c).This PWM block generates the sector1 (110).Saw tooth and timing signals are used to generate the PWM signals. Similarly it is easy to generate the PWM signals for the various other sectors namely 100,101,001,011,010.output of this PWM sector1 will be P_{0+},P_{0-}, A_+, A_-, B_+, B_-, C_+, C_-.These signals are fed to the OR gate units. Besides this OR gates will form the pulses which is required for the inverter unit. In order to form the pulse, OR gate is spitted into two groups. One is positive group and another one will be the negative group.

D.Three phase inverter block:

Three phase inverter block is obtained from the simulink library which is available in the matlab software. Input for this inverter is dc supply. Pulses which are required to operate this inverter are obtained from the pulse generation block which is working under SVPWM technique. This three phase inverter block delivers the three phase output voltage which is required for the star connected resistive and capacitive (RC) load.

SIMULATION RESULTS OF SVPWM

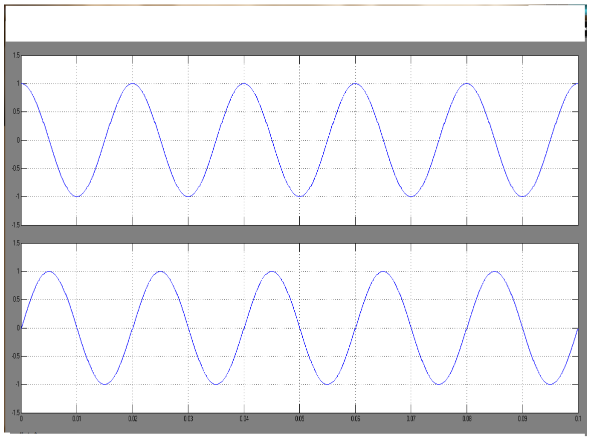
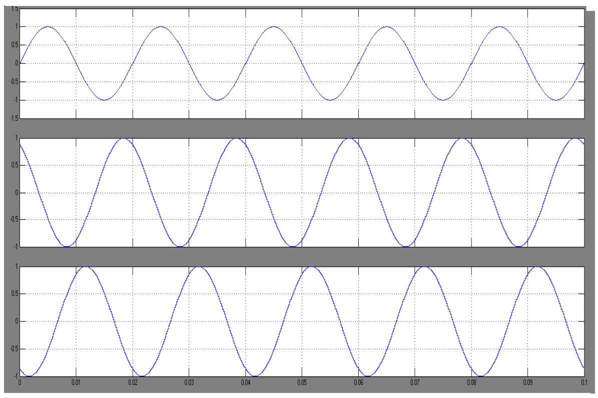


Fig (d) Alpha-beta signal.

Alpha beta signal is shown in fig(d).In this first figure represents alpha signal.This signal is cosine with the frequency of 50Hz.Second figure of fig (d) represents beta signal.This is sinusoidal signal with the frequency of 50Hz.



Fig(e)B1 B2 B3 signal.

Alpha-beta signal is shown in fig(d).From this alpha-beta signal B1,B2 and B3 signals are formed.These B1,B2,B3 are shown in fig(e).This signals are used to form the sectors.

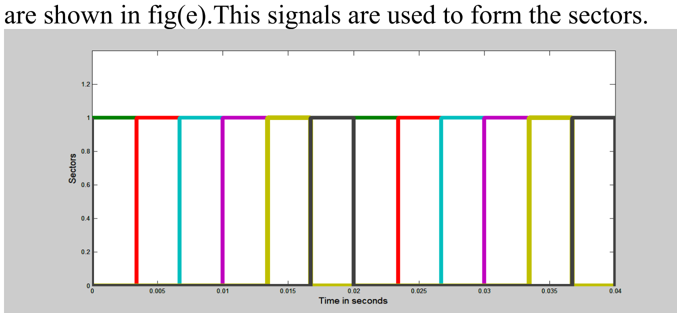


Fig (f) Sector formation.

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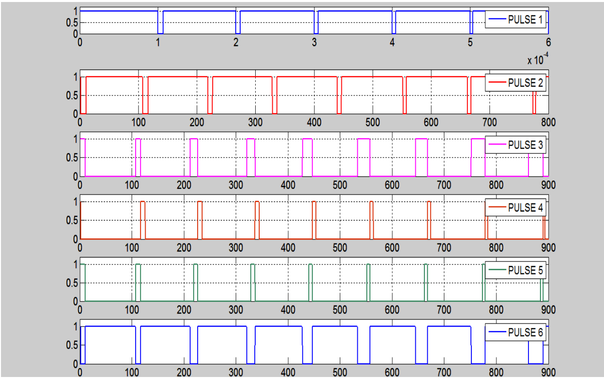
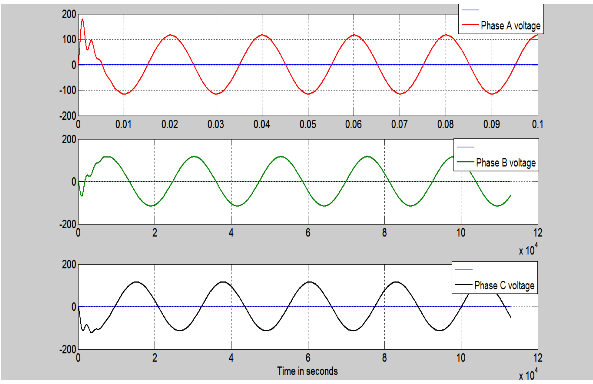
Sector formation is shown in fig (f).In this figure from top to bottom six sectors is there. These sectors are formed in the regular intervals. Pulse generation is mainly based on these sector formations. Therefore it plays a vital role in pulse generation.



Time in seconds

Fig (g) Pulse generation by svpwm technique.

Pulse generation is shown in fig (g) .Pulses are generated based on the inverter bridge firing strategy. From top to bottom of fig(g),six pulses are there. Pulses are given with the names Pulse 1, pulse 2, pulse 3, pulse 4, pulse 5, and pulse 6. ON time and OFF time these pulses are decided based on the firing requirements of the three phase inverter.



Fig(h)Phase-A,Phase-B and Phase-C voltages

Phase-A, phase-B and phase-C voltages are shown in fig (h). These voltage waveforms are taken between phases to neutral terminal of the load. By seeing this phase voltage waveforms, it is easy to identify the magnitude of the voltage.100V ac is delivered by this three phase inverter. For getting this 100V ac, 200V dc is given as input to the inverter by the battery unit. Moreover reference signal which is used in this svpwm unit is 0 to 1V dc.If reference dc is 1V, and then only 200V dc is converted to 100V ac.Therefore, in this svpwm unit reference dc plays a vital role.

TABLE FOR INVERTER OUTPUT WITH THD

Reference DC voltage in volts	DC Input to inverter by Battery unit in volts	Three phase inverter AC output voltage in volts	THD in percentage
0	200	0	0
0.25	200	29	0.412
0.5	200	58	0.393
0.75	200	87	0.391
1	200	100	0.389

Table 2: INVERTER OUTPUT WITH THD

Table 2 shows the variation of inverter output voltage with respect to reference DC voltage variation and also it shows the value of the total harmonic distortion of the inverter output. Initially, DC Input to inverter is fixed by battery as 200V.Then reference DC voltage is given as 0Volts.For this case, three phase inverter AC output voltage is 0Volts. Total harmonic distortion of this 0V is 0 percentage. If reference DC voltage is given as 0.25V, then inverter AC output voltage is 29V.In this case, total harmonic distortion will be 0.412. If reference DC voltage is given as 0.5V, then the inverter AC output voltage is 58V. In this case, total harmonic distortion will be 0.393.If reference DC voltage is given as 0.75V, and then the inverter AC output voltage is 87V. In this case, total harmonic distortion will be 0.391.If reference DC voltage is given as 1V, and then the inverter AC output voltage is 100V. In this case, total harmonic distortion will be 0.389.Therefore,from this table, it is clear that for 1V DC reference maximum level of inverter output will be 100Vand the corresponding harmonics is also very low compared to other cases.

IV. CONCLUSION

SVPWM model is simulated in the matlab environment. Six different sectors are formed by using alpha beta signal which is given as input. These different sectors are accurate. Moreover pulses are generated with uniform interval and it is following the SVPWM principle very clearly. Therefore the simulated outputs from the SVPWM model are delivering rated voltage for the star connected load. Besides total harmonic distortion of this inverter is quite low. In future, SVPWM principle will be implemented with three phase motor load and also hardware realization for this setup will be implemented.

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