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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Information Science and Engineering

Semester End Examination; March - 2021

Digital Design

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: Apply the principles of Boolean algebra/K - Map to manipulate and minimize logic expressions/functions.

CO2: Analyze and design Arithmetic Circuits and Data processing Circuits.

CO3: Design different units that are elements of typical computer's CPU using VHDL.

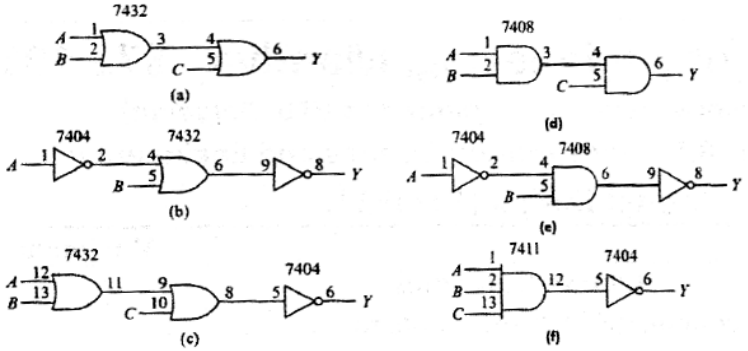
CO4: Design logic circuits using flip-flops/latches/registers.

CO5: Analyze and design Asynchronous and Synchronous Sequential circuits.

Note: ***I) PART - A*** *is compulsory.* ***Two*** *marks for each question.*

II) PART - B*: Answer any* ***Two*** *sub questions (from a, b, c) for Maximum of* ***18 marks*** *from each unit.*

Q. No.	Questions	Marks	BLs	COs	POs
	I: PART - A	**10**			
1 a.	Draw the logic circuit, whose Boolean equation is $Y = \overline{A+B} + \overline{C}$.	2	L1	CO1	PO1
b.	Draw the logic symbol for an Exclusive-OR gate.	2	L1	CO2	PO1
c.	Define Flip flop.	2	L1	CO3	PO1
d.	Define serial shifting and parallel shifting.	2	L1	CO4	PO1
e.	Define excitation map.	2	L1	CO5	PO1
	II: PART - B	**90**			
	UNIT - I	**18**			
1 a.	i) Perform the following operations (show the step by step calculation). I) $(463.25)_{10}$ = ( ) 2 II) $(36.25)_{10}$ = ( ) 8 III) $(AF9.0C)_{16}$ = ( )2 ii) Why NAND and NOR gates are called as universal gates? Explain with example.	9	L3	CO1	PO1
b.	Simplify the expression using Karnaugh map method; $F(A, B, C, D) = \Sigma m(1, 2, 3, 8, 9, 10, 11, 14) + d(7, 15)$	9	L3	CO1	PO2
c.	Construct the truth table and write the Boolean expression for the following logic circuits.	9	L3	CO1	PO2



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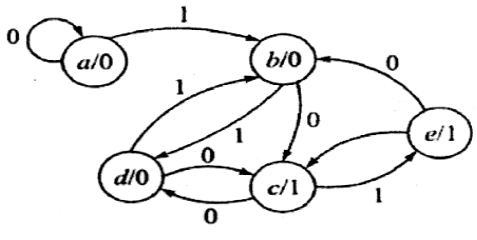
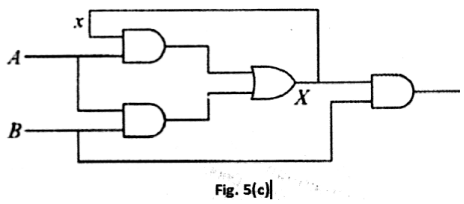
	UNIT - II	**18**			
2 a.	Simplify the following functions using Quine McCluskey method and realize expression using gates; $F(A, B, C, D) = \Sigma(0, 5, 7, 8, 9, 10, 11, 14, 15)$	9	L3	CO2	PO2
b.	Define Multiplexer. Explain 8-to-1 multiplexer with neat circuit diagram and truth table. Design 8-to-1 multiplexer using 4-to-1 multiplexer.	9	L2	CO2	PO1
c.	With the help of circuit diagram, explain Programmable Array logic and Programmable Logic Array and Programmable Read only Memory.	9	L2	CO2	PO1
	UNIT - III	**18**			
3 a.	Explain Half adder and Full Adder.	9	L2	CO3	PO1
b.	Explain clocked SR flip flop and JK flip flop with neat circuit diagram and timing diagram.	9	L2	CO3	PO1
c.	Derive the characteristic equation, draw state transition diagram and excitation table of the SR, JK, D and T Flip flops. Implement SR flip flop using JK flip-flop.	9	L2	CO3	PO1
	UNIT - IV	**18**			
4 a.	With a neat diagram and truth table, explain 4-bit SIPO shift register to store binary number 1011.	9	L2	CO4	PO1
b.	Explain Ring counter and Johnson counter.	9	L2	CO4	PO1
c.	Show a method for constructing a Mod-10 decade counter.	9	L2	CO4	PO1
	UNIT - V	**18**			
5 a.	Differentiate between Moore model and Melay model with appropriate state transition diagrams.	9	L2	CO5	PO1
b.	Reduce state transition diagram (Moore Model) of Fig. 5b by row elimination method and implication table method.  Fig. 5(b)	9	L3	CO5	PO2
c.	Analyze the Melay model asynchronous sequential circuit of Fig. 5(c) and show its stable state and corresponding outputs. And also give the state diagram of this circuit.  Fig. 5(c)	9	L3	CO5	PO2

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