U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; April / May -2021

CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: To acquire the knowledge of MOSFETs Characteristics, Fabrication Process, Combinational, sequential, dynamic circuits, Semiconductor Memories.

CO2: To Discuss the Techniques to estimate the delay and Power in MOSFETs.

CO3: To design combinational, sequential and Dynamic logic circuits based on CMOS for the given specifications.

CO4: To Analyse the issues, challenges, models, methodologies in CMOS Fabrication Process.

Note: I) *Answer any* ***FIVE*** *full questions, selecting* ***ONE*** *full question from each unit.*

II) *Any* ***THREE*** *units will have internal choice and remaining* ***TWO*** *unit questions are compulsory.*

III) *Each unit carries 20 marks.*

Q. No.	UNIT – I	Marks	BL	COs	POs
1 a.	Derive the expression for I_{ds} of long channel MOSFET in different regions.	10	L2	CO1	PO5
b.	Explain the following second order affects in MOSFET: i) Mobility degradation and Velocity saturation ii) Channel length modulation iii) Body effect	10	L4	CO4	PO3,5
	OR				
1 d.	Explain the DC characteristics of the CMOS inverter with different regions of operation.	10	L2	CO1	PO5
e.	Derive an expression for NM_L and NM_H.	5	L2	CO1	PO5
f.	Discuss Photolithography process in CMOS fabrication.	5	L2	CO1	PO5
	UNIT - II				
2 a.	Discuss the Linear delay model, Logic effort and Parasitic delay.	10	L3	CO2	PO3,5
b.	Explain the equivalent RC circuits of an inverter and transient response of first order RC system.	10	L3	CO2	PO3,5
	OR				
d.	Explain activity factor of dynamic power in MOSFETs.	10	L3	CO2	PO3,5
e.	Discuss static source in MOSFETs.	10	L3	CO2	PO3,5
	UNIT - III				
3 a.	Design the function $F = \overline{A + BC}$ using static CMOS and domino logic.	10	L6	CO3	PO3,5
b.	Design 2-input NAND gate using cascade voltage switch logic and dynamic circuit with footed and unfooted dynamic gates.	10	L6	CO3	PO3,5

Contd…2

UNIT - IV

4 a.	Develop CMOS implementation of a falling edge triggered master slave based D latch and briefly explain.	10	L6	CO3	PO3,5
b.	Explain sequencing methods in sequencing static circuits.	10	L2	CO1	PO3,5

OR

4 d.	What is pass transistor? Describe how logic '0' transfer place in pass transistor.	10	L3	CO1	PO5
e.	Explain the operation of voltage bootstrapping with suitable circuit and equation.	10	L3	CO1	PO5

UNIT - V

5 a.	What is Latch up in bulk CMOS devices? Explain with relevant diagram. Suggest method to prevent Latch up.	12	L4	CO4	PO3,5
b.	Explain 6T SRAM cell using CMOS.	8	L3	CO1	PO5

* * * *