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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Eighth Semester, B. E. - Electronics and Communication Engineering

Semester End Examination; July - 2021

Algorithm for VLSI Physical Design Automation

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer any **FIVE** full questions.*

1	a.	With a neat diagram, explain the several stages involved in VLSI physical design cycle.	10
	b.	Discuss the design style of full custom structure with necessary diagrams.	10
2	a.	Explain the fabrication process in detail.	10
	b.	Discuss size rules and separation rules followed in VLSI design rules.	6
	c.	Write the layout of a CMOS inverter.	4
3	a.	Discuss the issues of interconnect delay and parasitic effects in the fabrication process.	10
	b.	Discuss the innovative solutions to overcome the interconnect problems.	10
4	a.	Explain the following terminologies: i) Graph ii) Directed graph iii) Hyper graph iv) Bipartite graph v) Planar graph	10
	b.	Explain the list of atomic operation supported by a layout editor.	10
5	a.	Explain Kernighan-Lin algorithm in detail.	10
	b.	Explain simulated annealing algorithm in detail.	10
6	a.	Explain channel pin assignment.	10
	b.	What is rectangular dualization based floor planning? Explain with necessary diagrams.	10
7	a.	Explain Lee's algorithm to find the path between two vertices on the planar rectangular grid.	10
	b.	Explain the HADLOCK's algorithm with example.	10
8	a.	Explain how constraint graph is generated by shadow propagation algorithm?	10
	b.	Discuss two-dimensional compaction.	10
9	a.	Discuss geometric matching algorthm for clock routing with diagram.	10
	b.	Compute the delay calcuation for buffered and unbuffered clock trees.	10
10	a.	Explain the routing networks present in FPGA architecture.	10
	b.	Explain the routing algorithm for staggered model.	10

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