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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; Jan. - 2020

CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Analyze the impact of second order effect on the device performance with respect to,
i) Body effect
ii) Mobility variation
iii) Punch through effect — 8

b. Along with VTC and current waveform analyze the inverter design in all 5 regions of operation. — 12

2 a. Analyze the impact of second order effect on the device performance with respect to,
i) Tunneling
ii) Hot electron effect — 6

b. Obtain the small signal equivalent of MOSFET and comment on resistance variations. — 6

c. Obtain the capacitance model of MOSFET. — 8

UNIT - II

3 a. Obtain the schematic for the function $Y = \overline{(AB+C)D}$, using;
i) CMOS ii)Transmission gates — 6

b. Obtain the expression for V_{OL} and V_{OH} with respect to resistive load nmos inverter along with schematic and VTC. — 14

4 a. Analyze, alternate forms of pull-up's used in realizing nmos inverter along with VTC. — 12

b. Why CMOS inverter is preferred over nmos? Obtain the response curve if,
i) $\beta_n = \beta_p$ ii) $\beta_n \neq \beta_p$ — 8

UNIT - III

5 a. Analyze the performance of SR latch along with schematic and timing diagram. — 6

b. Obtain the expression for C_{boot} using voltage boot strapping principle. — 6

c. Analyze the basic principle employed in static RAM with necessary diagram. — 8

6 a. Analyze the performance of CMOS D latch along with schematic and timing diagram. — 6

b. "Dynamic CMOS logic circuits cannot be cascaded''. Justify. — 6

c. Analyze the basic operation of dynamic RAM along with necessary diagram. — 8

Contd….2

UNIT - IV

7	a.	List and discuss the causes and remedies of latch–up in *n*-well CMOS inverter.	12
	b.	Analyze the charge sharing phenomenon in dynamic CMOS circuits.	8
8	a.	Realize the pipeline architecture using Domino CMOS structure.	10
	b.	Obtain the various techniques employed for clock generation.	10

UNIT - V

9	a.	Analyze the LDD refractory gate in current CMOS technology.	8
	b.	Realize the schematic and the stick diagram (Using CMOS) for the function, $Y = \overline{A + BC}$.	6
	c.	Obtain the delay expression in; i) NMOS inverter ii) CMOS inverter	6
10	a.	Analyze the performance of multilayer connect in current CMOS technology.	6
	b.	Realize the schematic and symbolic layout for the function, $Y = \overline{AB + CD}$.	6
	c.	Obtain the expression for propagation delay in a cascaded network of varying sizes.	8

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