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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; Jan. - 2020

SOC Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Compare SOC, SIP and SOB on different characteristics. 10

b. Outline the SOC design flow procedure.

2 a. What is SOC? Also discuss the SOC Bottlenecks, Opportunities and Challenges of current generation SOC design with special emphasis on Moore's law. 10

b. What are important specifications of SOC design process? Explain types of SIC specification. 10

UNIT - II

3 a. Differentiate between;

i) Microcontrollers and Microprocessors 10

ii) RISC versus CISC

b. Write short note on;

i) Von-Neumann architecture 10

ii) Interrupt architectures

4 a. Explain MESI protocol with its state diagram. 6

b. What is flash memory? Explain NOR flash memory cell and compare with NAND flash memory cell. 7

c. Draw cache system architecture and discuss the cache mapping technologies. What is cache coherence? 7

UNIT - III

5 a. What is network on chip? Explain direct, indirect and Hybrid topologies with a neat diagram. 10

b. What is the need for hardware accelerator in SOC? What are the tradeoffs in implementing these functionalities in SOC? 10

6 a. Discuss limitations of bus based architecture and explain different bus topologies. 10

b. What are the different switching strategies in NOC? Explain Worm hole switching. 10

UNIT - IV

7 a. Explain heterodyne down conversion receivers with block diagrams. Also discuss the issue in image rejection. 10

b. Explain the principle of pipeline ADC and derive an expression for DNL max. 10

Contd…2

8 a. Explain the block diagram of Hartley image rejection receiver, and how the image band is rejected? Explain it. 10

b. Justify the need for sensors and amplifiers in SOCs. 10

UNIT - V

9 a. Describe HW-SW co-design with suitable example. Also discuss the challenges and opportunities for co-design in current generation SOC design. 10

b. With neat flow chart, explain high level verifications for SOC devices. 10

10 a. Write short notes on the following:

i) ESL design flow 10

ii) Hard and Soft IP

b. What is the need for power management in SOC? What are the different sources of power dissipation? 10

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