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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; Dec - 2019

VLSI Functional Verification Using System Verilog

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1	a.	Analyze the different kinds of register types (any 5) with general format and example.	10
	b.	Write the gates level descriptions of 2 to 4 decoder along with the circuit.	5
	c.	Write a Verilog code for 9 bit parity generator.	5
2	a.	Analyze the various operators in Verilog HDL showing precedence and names.	10
	b.	Write gate level descriptions of 4 to 1 multiplexer.	5
	c.	Realize 4:2 line priority encoder and write the gate level description.	5

UNIT - II

3	a.	Using edge triggered D flip flop, write a Verilog HDL description for 4 bit register.	5
	b.	Write a Verilog HDL model for master slave flip flop (D type) using assign statement.	5
	c.	Bring out the differences between continuous assignment and procedural assignment.	10
4	a.	How is combinational UDP differing from a sequential UDP?	6
	b.	Develop a Verilog model and write the Verilog HDL for 8 bit magnitude comparator.	6
	c.	How does casex statement differ from the case statement? Explain with an example.	8

UNIT - III

5	a.	Design and develop Verilog module for full adder using half adder modules.	10
	b.	Write a Verilog module using always statement to generate a clock with t_{on} = 5 ns, t_{off} = 2 ns.	6
	c.	Develop a Verilog module for level sensitive D flip flop using wait statement.	4
6	a.	Write a structural Verilog HDL for a decade counter using JK flip flop.	8
	b.	Justify, Transport delay can be modeled using non-blocking assignment, with example.	6
	c.	Write a Verilog code for gated SR latch.	6

UNIT - IV

7	a.	Explain the constrained random test coverage.	6
	b.	Bring out the difference between test progress with and without feedback.	8
	c.	Analyze simplified layered test bench with relevant block diagram.	6
8	a.	Analyze various methodology basic applicable for verification process.	8
	b.	Explain the various test bench components.	6
	c.	Analyze the simple generator class with general format.	6

UNIT - V

9	a.	Explain the coverage flow with relevant diagram.	10
	b.	Analyze test bench with virtual interfaces.	10
10	a.	Explain the impact of functional coverage on code coverage to measure completeness.	10
	b.	Design and develop Verilog model of an interface with serial protocol to a test bench.	10

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