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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; Jan. - 2020

Digital System Design Using Verilog

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1	a.	Discuss the important properties and constraints of real world circuits.	12
	b.	Describe the design methodology for hardware and software co-design with flowchart.	8
2	a.	Explain parity tree circuit diagram for generating and checking even parity for as 8-bit code.	8
	b.	Develop Verilog module for 7-segment decoder.	6
	c.	Develop Verilog model for a 4:1 multiplexer in gate-level modeling.	6

UNIT - II

3	a.	Explain the operation of resizing unsigned integers.	6
	b.	Explain fast carry chain full adder cells with diagrams.	8
	c.	Develop a Verilog model of a code converter to convert the 4-bit gray code to a 4-bit unsigned binary integer.	6
4	a.	Explain the implementation of shift register using D-flip flop and multiplexers.	6
	b.	Design and develop a Verilog model for modulo 10 counter (Decode counter).	8
	c.	Differentiate between Melay and Moore machine model.	6

UNIT - III

5	a.	Determine whether there is an error in the ECC word 000111000100 and if, so, correct it.	8
	b.	Discuss multiport memories in detail.	8
	c.	Draw 1-bit dynamic circuit and analyze it's working.	4
6	a.	Design 64k×8 bit composite memory with four 16k×8 bit components and explain.	12
	b.	Write the internal organization of a CPLD and explain.	8

UNIT - IV

7	a.	Explain with block diagram, the organization of high performance embedded computer with multiple buses.	8
	b.	Write a gum nut assembly language program to find the greater of two values.	8
	c.	What is meant by term Little-Endian and Big-Endian memory layout for data words?	4

Contd…2

8 a. Explain the following I/O synchronization techniques:

i) Interrupts

ii) Polling 8

b. Discuss different serial interface standards. 12

UNIT - V

9 a. With the help of block diagram, explain video edge detection. 8

b. Discuss pipelined organization of an accelerator. 6

c. What is functional design and verification? Discuss in detail. 6

10. Write a short notes on:

i) Area Optimization

ii) Timing Optimization

iii) Power Optimization

iv) Fault models and Simulation 20

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