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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Eighth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Aug. / Sep. - 2020

Algorithms for VLSI Physical Design Automation

Time: 3 hrs *Max. Marks: 100*

***Note**: i) Answer **TWO** full questions, selecting **ONE** full question from **UNIT - I** and **UNIT - II**.*
*ii) Answer any **THREE** full questions, choosing from **UNIT - III, UNIT - IV** and **UNIT - V**.*

UNIT - I

1 a. With neat diagram, discuss the steps involved in VLSI design cycle. 12

b. Compare between different styles with respect to uneven height cells, area performance and fabrication. 8

OR

2 a. Draw the schematic and layout for a CMOS NAND gate. 4

b. Explain DRAM. 8

c. State different basic steps in MOS fabrication process. 8

UNIT - II

3 a. List the issues related to the fabrication process. 4

b. Compare different fabrication process. 6

c. Write a note on; 10

i) Noise and Crosstalk ii) Interconnect delay

OR

4 a. What do you mean by NP hardness problems? List the algorithms, which solve NP hardness problems. 5

b. List the basic algorithms for MST? Explain single pair and all pair shortest paths. Also explain shortest path algorithm. 10

c. List the atomic operations that a layout editor must support. 5

UNIT - III

5 a. List the different varieties of classification of partitioning algorithms? Explain. 8

b. Explain K-L algorithm and also list extension. 12

6 a. Explain integer programming algorithm for floor planning. 12

b. Discuss the sequence-pair technique. 8

UNIT - IV

7 a. Write the Souk Up-Router algorithm. 6

b. Mention all net types and routing patterns for a routing graph. 8

c. Explain shortest path algorithm. 6

Contd...2

8 a. With an example, explain constraint graph based compaction. 10

b. Explain 2-D compaction. 10

UNIT - V

9 a. State MMM algorithm in detail. 10

b. Write a note on Power and Ground routing. 10

10 a. Explain the type and routing models of FPGA technologies. 10

b. State graph expansion algorithm. 5

c. Explain physical design cycle for FPGAs. 5

2.7.2020

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