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P.E.S. College of Engineering, Mandya - 571 401
(An Autonomous Institution affiliated to VTU, Belagavi)
First Semester, M. Tech - VLSI Design and Embedded System (MECE)
Semester End Examination; April / July - 2021
Embedded System Design

Time: 3 hrs   *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: To gain knowledge of components of Embedded systems such as system core, I/O devices, memory, communication interface, multiprocessing, and RTOS.

CO2: To obtain insight to design challenges, techniques, methodology, debugging techniques, performance criteria and non-functional requirements.

CO3: To be able to design simple Embedded systems for the practical problems and debug/test them. Also, able to prepare & present a report.

CO4: To be able to analyze Embedded systems and related issues and come up with improvised solutions through self learning and research.

<u>*Note:*</u> *I) Answer any **FIVE** full questions, selecting **ONE** full question from each unit.*

*II) Any **THREE** units will have internal choice and remaining **TWO** unit questions are compulsory.*

III) Each unit carries 20 marks.

Q. No.	UNIT - I	Marks	BLs	COs	POs
1 a.	Considering GPS moving map system as an example, discuss its requirement analysis and architecture design.	10	L2	CO4	PO5
b.	Discuss ARM7 programming model and data instructions with example.	10	L3	CO2	PO3
	OR				
1 d.	Discuss generalization, inheritance and link as applicable to UML with illustrations.	10	L2	CO2	PO3
e.	Discuss design challenges and performance of embedded systems.	10	L2	CO4	PO5
	UNIT - II				
2 a.	Discuss the different methods of mapping and communicating I/O devices with processor.	10	L3	CO2	PO5
b.	Explain importance and operation of Direct Memory Access (DMA) with suitable block diagram and UML sequence diagram.	10	L3	CO2	PO5
	OR				
2 d.	Explain four cycle handshake mechanism in communicating among the devices with necessary diagram.	5	L3	CO2	PO5
e.	Explain read operation in Synchronous Dynamic RAM (SDRAM) with required timing diagram.	5	L3	CO2	PO5
f.	Explain direct mapped and set associative cache techniques and make a comparison of the two.	10	L3	CO4	PO5

UNIT - III

3 a.	Discuss the different debugging techniques and debugging challenges.	8	L2 CO2 PO3	
b.	Explain 'Black box' testing method used in program validation and testing.	6	L2 CO2 PO5	
c.	Discuss basic loop optimization used in optimizing software performance.	6	L2 CO2 PO5	

UNIT - IV

4 a.	Differentiate between 'Racing', 'Deadlock' and 'Livelock' conditions. Discuss methods to handle 'Deadlock' condition.	10	L3 CO4 PO5	
b.	Three processes with ID's P_1, P_2, P_3 with Estimated Completion Time (ECT) 10, 6, 8 ms and priorities 2, 4, 3 respectively enter the ready queue together. A new process P_4 with ECT 6 ms and priority 0 enter the 'Ready' queue after 5 ms of start of execution of first process and an another process P_5 with ECT 4 ms and priority 1 enters 'Ready' queue after 10 ms of start of execution process of first process. Assume all the processes contain only CPU operation and I/O operation are involved. Compute Wait time, Turn Around Time (TAT) for each process, if priority based preemption scheduling algorithm is used.	10	L3 CO4 PO5	

OR

4 d.	Define Multi-tasking. Discuss types of multi-tasking and factors considered in choosing scheduling algorithm.	10	L2 CO1 PO5	
e.	Explain 'mailbox' and 'signalling' techniques used in inter-process communication.	5	L2 CO1 PO5	
f.	Two processes with ID's P_1 and P_2 and ECT 12, 4 ms respectively enters the 'Ready' queue together. Calculate the waiting time and TAT for each process and average waiting time and TAT (assume there is no I/O waiting for the processes) in shortest job first scheduling algorithm.	5	L3 CO4 PO5	

UNIT - V

5 a.	Explain waterfall and spiral model used with software development.	8	L2 CO1 PO5	
b.	Discuss two major types of multiprocessor architectures with necessary diagram.	6	L2 CO1 PO5	
c.	Discuss role and importance of accelerators in performance enhancement.	6	L2 CO1 PO5	

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