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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; April / July - 2021

Physical Design

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: To apply the knowledge of graph theory in VLSI Physical Design.

CO2: To be able to analyze the VLSI Physical Design algorithms.

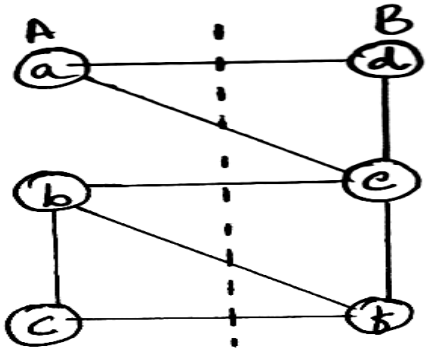
CO3: To be able to apply the VLSI Physical Design algorithms.

CO4: To be able to analyze the Physical Design for specific constraints.

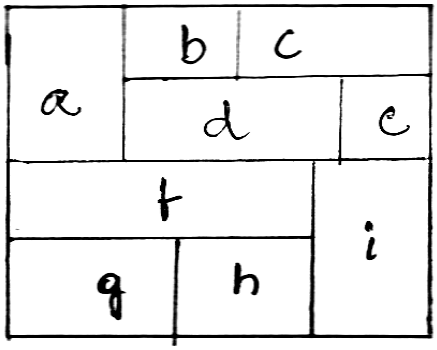
Note: I) *Answer any* ***FIVE*** *full questions, selecting* ***ONE*** *full question from each unit.*

II) *Any* ***THREE*** *units will have internal choice and remaining* ***TWO*** *unit questions are compulsory.*

III) *Each unit carries 20 marks.* ***IV)*** *Missing data, if any, may suitably be assumed.*

Q. No.	UNIT - I	Marks	BLs	COs	POs
1a.	Briefly explain VLSI design styles in physical style design.	10	L2	CO2	PO5
b.	Given the initial partition of nodes (*a* - *f*) as shown in figure can be optimally partitioned using KL algorithm. Perform the first pass of the algorithm. The dotted line represents the initial partitioning. 	10	L2	CO1	PO3

UNIT - II

2 a.	Illustrate the pin assignment along with example in chip planning.	8	L4	CO2	PO5
b.	For the given floor-plan shown in figure, generate its slicing tree, vertical constraint graph and horizontal constraint graph. 	4	L4	CO2	PO5

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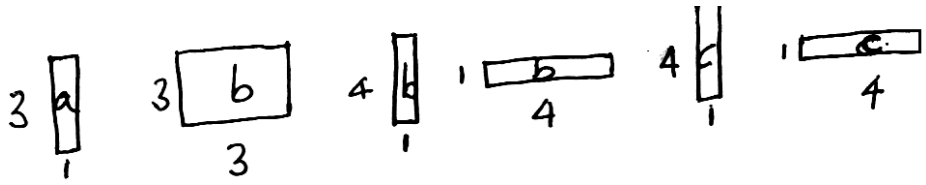
c. Three blocks *a*, *b*, and *c* given along with their size options as shown in figure.

i) Determine shape functions for each block *a*, *b*, *c*

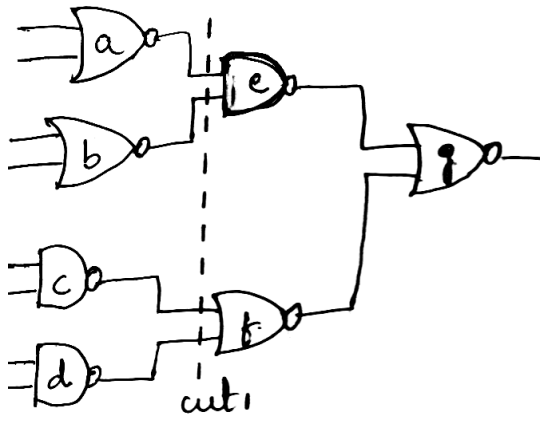
ii) Find the minimum area of the floor-plan using both horizontal and vertical composition and its corresponding slicing tree — 8 L2 CO3 PO1



UNIT - III

3 a. Illustrate the rectilinear routing in global routing. 10 L4 CO2 PO5

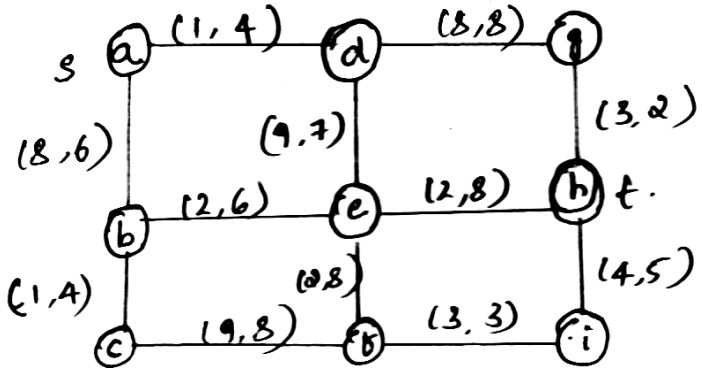
b. Perform min-cut placement to place gates *a* - *g* on a 2× 4 grid as shown in figure. Use Kernighan-Lin algorithm for partitioning. Use alternating cutline's. The cutline cut1 represents the initial vertical cut. Each edge on grid has capacity $\sigma_p(e) = 2$. Estimate whether the placement is routable. 10 L2 CO3 PO1



OR

3 d. Discuss the optimization goals in global routing. 10 L2 CO2 PO5

e. For the graph with weighs (w_1, w_2) as shown below figure. Use Dijkstra's algorithm to find a minimum cost path from the starting node *s* = *a* to the target node *t* = *i* generate table for groups 2 and 3. 10 L2 CO3 PO1



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UNIT - IV

4 a.	Illustrate geometric matching based algorithm.	5	L4	CO2	PO5
b.	Briefly explain multiple clock routing.	6	L2	CO1	PO5
c.	Illustrate DME algorithm.	9	L4	CO2	PO5

OR

4 d.	Discuss design style specific problems on clock routing.	6	L2	CO1	PO3
e.	Briefly explain skew and delay reduction by pin assignment.	6	L2	CO2	PO5
f.	Illustrate the H-tree based algorithm.	8	L4	CO2	PO5

UNIT - V

5 a.	Illustrate delay budgeting with zero slack algorithms.	10	L4	CO4	PO3
b.	Illustrate timing driven placement in timing closure.	10	L4	CO4	PO5

OR

5 d.	Briefly explain net list restructuring in physical synthesis.	10	L2	CO4	PO5
e.	Illustrate performance driven design flow in timing closure.	10	L4	CO4	PO3

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