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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; April / July - 2021

Digital System Design Using Verilog

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: To gain knowledge of Verilog modeling in term of digital system and Embedded systems.

CO2: To obtain insight to design challenges, techniques, methodology, performance criteria and design flow.

CO3: To be able to design and develop Verilog model of digital logic circuits and simple Embedded systems applications, prepare and present a report.

CO4: To be able analyze synthesis report of digital logic circuits and come up with optimized design through self learning and research.

Note: I) *Answer any* ***FIVE*** *full questions, selecting* ***ONE*** *full question from each unit.*

II) *Any* ***THREE*** *units will have internal choice and remaining* ***TWO*** *unit questions are compulsory.*

III) *Each unit carries 20 marks.* ***IV)*** *Missing data, if any, may suitably be assumed.*

Q. No.	UNIT - I	Marks	BLs	COs	POs
1a.	Describe the design methodology for hardware and software co-design with flowchart.	10	L1	CO1	PO5
b.	Discuss BCD code and 7 segment decoder.	6	L3	CO1	PO5
c.	Develop a verilog model for a 4-to-1 multiplexer.	4	L3	CO1	PO5
	UNIT - II				
2 a.	Explain the operation of resizing unsigned integers.	6	L2	CO2	PO3,5
b.	Design a circuit that counts 16 clock cycles and produces a control signal, ctrl, that is 1 during every eight and twelth cycle.	8	L3	CO2	PO3,5
c.	Design a circuit for a Modulo-10 counter, otherwise known as a decode counter.	6	L3	CO2	PO3,5
	UNIT - III				
3 a.	Design a 64k × 8-bit composite memory using four 16k × 8-bit components.	8	L3	CO3	PO2,3,5
b.	Develop a verilog model of a dual-port, 4k × 16-bit flow through SSRAM. One port allows data to be written and read, while the other port only allows data to be read.	8	L3	CO3	PO2,3,5
c.	Explain the synchronous static RAM with timing diagram.	4	L2	CO3	PO2,3,5
	OR				
3 d.	Discuss in detail the multiport memories.	6	L2	CO2,3	
e.	Discuss an internal organization of CPLD.	10	L2	CO2,3	
f.	Describe differential signaling. How does it improve noise immunity?	4	L1	CO3	

Contd… 2

UNIT - IV

4 a.	Design and synthesize of a sequence recognizer.	10	L4	CO4	PO5
b.	Develop and synthesize of a Moore type NRZ to Manchester line code counter.	10	L4	CO4	PO5

OR

4 d.	Design and synthesize a sequential machine whose inputs are clock and reset and whose outputs are clk_by_6 and clk_by_10 (i.e, clock divider outputs that divide clk_by_6 and 10 respectively).	10	L4	CO4	PO5
e.	Develop, verify and synthesize a frequency divider with programmable divisor for the base frequency and a programmable duty cycle.	10	L4	CO4	PO5

UNIT - V

5 a.	Develop, verify and synthesize count gray-bin, a 4-bit counter that can count in gray or in binary code, depending on an input mode.	10	L4	CO4	PO5
b.	Discuss how to describe a synchronous reset condition using verilog?	10	L4	CO4	PO5

OR

5 d.	Design the architecture of synchronous 4-bit binary counter.	10	L4	CO4	PO5
e.	Explain the partitioned sequential machine.	10	L4	CO4	PO5

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