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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; April / July - 2021

SOC Design

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: To Memorize the system architecture, components of system hardware and software, external and internal memory of SOC and organization, interconnect architectures Like AMBA, NOC.

CO2: To gain the knowledge of processor architecture, instructions, delays for the optimised solution, reconfigurable device, error detection and correction.

CO3: To be able to understand the applications of System on Chip, prepare and present a report.

CO4: To be able to apply the knowledge gained in system on chip for the optimization of time, area, power, reliability, configurability, memory design and interconnect architectures through self learning and research.

Note: I) *Answer any* ***FIVE*** *full questions, selecting* ***ONE*** *full question from each unit.*

II) *Any* ***THREE*** *units will have internal choice and remaining* ***TWO*** *unit questions are compulsory.*

III) *Each unit carries 20 marks.* ***IV)*** *Missing data, if any, may suitably be assumed.*

Q. No.	UNIT - I	Marks	BLs	CO	PO
1a.	With the help of neat diagram, discuss processor architecture and its implementation.	8	L1	CO1	PO5
b.	Explain basis SOC System model and give example of its applications.	8	L2	CO2	PO3
c.	List SOC software and hardware design benefits and its drawbacks.	4	L3	CO3	PO2
	OR				
1 d.	Describe the operation of simple sequential and pipelined processor with the help of neat diagram.	10	L2	CO3	PO2
e.	Explain the vector processor model with the help of neat figure.	5	L2	CO3	PO2
f.	Explain with component model engineering cost for SOC development.	5	L1	CO1	PO5
	UNIT - II				
2 a.	Explain optimization of pipeline processor design.	8	L2	CO2	PO5
b.	Discuss the baseline floor plan and explain the summary of area design rules.	10	L3	CO4	PO3
c.	Describe scrubbing test.	2	L1	CO2	PO3
	OR				
2 d.	Describe the five basis SOC tradeoffs to provide a framework for analyzing SOC.	6	L2	CO2	PO3
e.	Describe how SOC dealt with physical faults?	10	L3	CO4	PO3
f.	Describe area-time power tradeoffs in processor design.	4	L1	CO2	PO3

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UNIT - III

3 a.	What are scratch pads and cache memory? Mention three principles involved in cache process.	8	L2	CO4	PO3
b.	Describe the cache organization.	10	L3	CO4	PO3
c.	Mention and explain three replacement policies that are widely used.	2	L1	CO4	PO3

OR

3 d.	Explain SOC internal memory with placements.	6	L3	CO4	PO3
e.	Write a block diagram of memory chip. With the waveform, explain DRAM chip timing.	8	L2	CO4	PO3
f.	Discuss the memory buffers.	6	L1	CO4	PO3

UNIT - IV

4 a.	Discuss a simplified block diagram of an SOC module in a system context.	6	L2	CO1	PO5
b.	Explain the concept of arbitration and protocols.	6	L1	CO1	PO5
c.	With the help of a neat diagram, explain the layered architecture of NOC and mention the number of benefits.	8	L2	CO3	PO2

UNIT - V

5 a.	What are three common means of implementing computations?	6	L3	CO2	PO3
b.	Describe the typical tool flow for an FPGA.	7	L3	CO2	PO5
c.	Explain with neat figure CUSTARD micro architecture showing threading register file, and forwarding network parameterization.	7	L2	CO4	PO3

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