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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fourth Semester, B. E. - Electronics and Communication Engineering

Semester End Examination; July / August - 2022

Digital Design Using Verilog HDL

Time: 3 hrs *Max. Marks: 100*

Course Outcome

The Students will be able to:
*CO1: To **apply** the knowledge of digital fundamentals to explain basic concepts used in Verilog HDL*
*CO2: To **write** a Verilog model for combinational and sequential circuits*
*CO3: To **analyse** the given digital circuit and develop Verilog model for given digital circuits.*
*CO4: To **design** any combinational and sequential circuits and develop Verilog model for the given inputs.*
*CO5: To **verify** the design through synthesis and demonstrate the application using EDA tools.*

Note: *i) **PART-A** is compulsory. One question from each unit for maximum of 2 marks.*
*ii) **PART-B** Answer any **TWO** sub questions (from a, b, c) from each unit for a Maximum of 18 marks.*

Q. No.	Questions	Marks	BLs	COs	POs
	I:PART - A	**10**			
I a.	Mention data types used in verilog HDL.	2	L3	CO1	PO1
b.	Any two differences between tasks and functions.	2	L2	CO1	PO1
c.	Write a switch diagram for 2:1 multiplexer.	2	L3	CO1	PO1
d.	Define logic synthesis.	2	L1	CO1	PO1
e.	Define the components of a traditional verification flow.	2	L2	CO1	PO1
	II:PART - B	**90**			
	UNIT - I	**18**			
1 a.	Explain system tasks relevant to verilog HDL.	9	L2	CO1	PO1
b.	Explain port declaration with an example using verilog code.	9	L2	CO1	PO1
c.	Define instantitation and instances? Write a verilog code for 4-bit ripple carry full adder to show instantitation and instances.	9	L1	CO1	PO1
	UNIT - II	**18**			
2 a.	Explain the blocking assignment statements and non-blocking assignment statements with relevant examples.	9	L2	CO1	PO1
b.	Write a note on the following loop statements: i) While loop ii) Forever loop	9	L2	CO1	PO1
c.	Explain sequential and parallel blocks with examples.	9	L2	CO1	PO1
	UNIT - III	**18**			
3 a.	Explain procedural continuous assignments with an example.	9	L2	CO1	PO1
b.	Explain different types of delay models with examples.	9	L2	CO1	PO1
c.	Develop the switch level verilog model stimulus for two inputs CMOS NOR gate.	9	L3	CO1	PO1

Contd…2

	UNIT - IV	**18**			
4 a.	Develop a verilog model and stimulus for 4:1 MUX with UDP.	9	L3	CO1	PO1
b.	Explain simulation flow using PLI routines.	9	L2	CO1	PO1
c.	Explain basic synthesis design flow from RTL description to gate level description.	9	L2	CO1	PO1
	UNIT - V	**18**			
5 a.	Develop a verilog model for RTL description for news paper vending machine FSM.	9	L3	CO1	PO1
b.	With block diagram, explain formal verification and assertion checking.	9	L2	CO1	PO1
c.	Briefly discuss the flow chart of traditional verification flow.	9	L3	CO1	PO1

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