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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Computer Science and Engineering

Semester End Examination; July / Aug. - 2022

Computer Architecture

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: Describe the evolution of computers.

CO2: Analyze the basic properties of pipelining.

CO3: Understand the Instruction Level Parallelism and Its Exploitation.

CO4: Discuss system architecture of multiprocessor and Thread Level Parallelism..

CO5: Analyze the steps to perform parallelization of computation.

***Note**: I) **PART - A** is compulsory. **Two** marks for each question.*

*II) **PART - B**: Answer any **Two** sub questions (from a, b, c) for a Maximum of **18 marks** from each unit.*

Q. No.		Questions	Marks	BLs	COs	POs
		I : PART - A	**10**			
I	a.	Explain the term module availability.	2	L2	CO1	1,2,3
	b.	What is pipelining?	2	L1	CO2	1,2,3,4
	c.	What is loop-level parallelism? Also write an example for the same.	2	L2	CO3	1,2,3,4
	d.	Explain the terms coherence and consistency.	2	L1	CO4	1,2,3,4
	e.	What are the major performance goals of the parallelization process?	2	L2	CO5	1,2,3,4
		II : PART - B	**90**			
		UNIT - I	**18**			
1	a.	Briefly explain the different classes of computers.	9	L2	CO1	1,2,3
	b.	Illustrate the seven dimensions of an instruction set architecture.	9	L3	CO1	1,2,3
	c.	Consider the following measurement: Frequency of FP operation = 25% Average CPI of FP operation = 4.0 Average CPI of other instruction of = 1.33 Frequency of FPSQR = 2% CPI of FPSQR – 20 Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operation to 2.5 compare these, two design alternatives using the processor performance equation.	9	L2	CO1	1,2,3
		UNIT - II	**18**			
2	a.	Describe the five basic clock cycles required to implement a MIPS instruction.	9	L2	CO2	1,2,3,4
	b.	Explain the five semi-independent axes on which exceptions can be characterized.	9	L2	CO2	1,2,3,4
	c.	Explain briefly the three different classes of pipeline hazards.	9	L2	CO2	1,2,3,4

Contd… 2

UNIT - III **18**

3 a. Assume a single-issue pipeline processor considering a loop unrolling factor of 3. Schedule the below code without any stalls by loop unrolling technique. Do not reuse any of the register

for (i = 0, i < 999; i++)
$x[i] = x[i] + s$;

Refer the below table for latencies of FP operation

9 L4 CO3 1,2,3,4

Instruction producing result	Instruction using Result	Literacy in clock cycles
FP ALU OP	FP ALU OP	3
FP ALU OP	Store Double	2
Load double	FP ALU OP	1
Load double	Store Double	0

b. Explain the basic structure of dynamic scheduling approach using Tomasulo's algorithm. Also illustrate the reservation station along with address tags, when all the below instruction have issued, but only first load has completed.

Execution and written its result to the CDB

9 L4 CO3 1,2,3,4

1. LD F_6, 32(R_2)
2. LD F_2, 55(R_3)
3. MUL.D F_0, F_2, F_4
4. SUB.D F_8, F_2, F_6
5. DIV.D F_{10}, F_0, F_6
6. ADD.D F_6, F_8, F_2

c. Illustrate instruction level parallelism with an example code. Consider the following code fragment for $Y = a * X + Y$ where 'a' is a scalar and '*X*' and '*Y*' are vectors.

Loop : LD F_0, a
DADDIU R_4, R_X, #512
LD F_2, O(R_X)
MUL.D F_2, F_2, F_0
LD F_4, O(R_Y)
ADD.D F_4, F_4, F_2
SD F_4, 9(R_Y)
DADDIU R_X, R_X, #8
DADDIU R_y, R_Y, #8
DSUBU R_{20}, R_4, R_X
BNEZ R_{20}, Loop

9 L4 CO3 1,2,3,4

List all the date dependencies in the above code. Answer in the following format register, source instruction and destination instruction.

Contd… 3

	UNIT - IV	**18**				
4 a.	Discuss directory based cache coherence for distributed memory multiprocessor system along with state transition diagram.	9	L2	CO4	1,2,3,4
b.	What is cache coherence problem in multiprocessor architecture? Explain how cache coherence problem can be solved by snooping coherence protocol.	9	L2	CO4	1,2,3
c.	Explain Symmetric Multiprocessors (SMP_s) and Distributed Shared Memory (DSM) with a neat diagram. And also write the difference between SMP_S and DSM.	9	L2	CO4	1,2,3
	UNIT - V	**18**				
5 a.	Explain the four different steps involved in creating a parallel program from a sequential one.	9	L2	CO5	1,2,3,4
b.	Write the pseudocode describing the sequential equation solver kernel.	9	L2	CO5	1,2,3,4
c.	With pseudocode, explain the orchestration of "equation solver" problem under data parallel model.	9	L2	CO5	1,2,3,4

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