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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Seventh Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; February - 2022

Low Power VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1	a.	Explain the different sources of Power dissipation.	5
	b.	Discuss the physics of power dissipation of MOSFET devices.	8
	c.	Explain the effects of influencing threshold voltage.	7
2	a.	Derive an equation for the short circuit power dissipation of an unloaded inverter.	8
	b.	List the hierarchy of limits and explain any two of them.	7
	c.	Discuss the Gate induced Drain leakage in MOSFET.	5

UNIT - II

3	a.	Explain the behavioral level transforms.	6
	b.	Illustrate how the computation is carried out in transposed direct form along with it signal flow graph?	7
	c.	Discuss the circuit activity driven architectural transformations.	7
4	a.	Discuss the power optimization using operation reduction.	6
	b.	Explain the FSM and combinational logic synthesis.	7
	c.	Discuss pre-computation architecture based optimization for low power.	7

UNIT - III

5	a.	Analyze the power consumption of CMOS gates for the function; $y = \overline{(x_1 + x_2)x_3}$.	7
	b.	Explain the terms: delay, power consumption, optimization algorithm with transistor reordering.	6
	c.	Explain the following with reference circuit level transform for power optimization: i) Gate delay model ii) Switching events probabilities	7
6	a.	Discuss the concept of NMOS and Pseudo nMOS logic.	8
	b.	Discuss the following in brief with necessary diagram: i) Pass Transistor Logic ii) Domino NAND Gate Logic	8
	c.	Define punchthrough and narrow width effect.	4

Contd... 2

UNIT - IV

7	a.	Discuss the organization of RAM.	6
	b.	Discuss the banking organization of SRAMs.	7
	c.	With a neat figure, explain the divided word line architecture.	7
8	a.	Discuss the energy dissipation in transistor channel using an RC model.	8
	b.	Explain the generic resonant scheme for adiabatic clock generation circuit.	12

UNIT - V

9	a.	Explain the sources of software power dissipation.	7
	b.	Describe the software power estimation at gate and architectural level.	7
	c.	Describe bus switching activity for software power estimation.	6
10	a.	Explain the software power optimization using algorithm transformation.	6
	b.	Define instruction level power analysis for software power optimization.	8
	c.	Explain power management for software optimization.	6

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