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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Computer Science and Engineering

Make-up Examination; May - 2022

Digital Logic Design

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: Design simplified logic circuits using Boolean equation minimization techniques.

CO2: Design the data processing circuits.

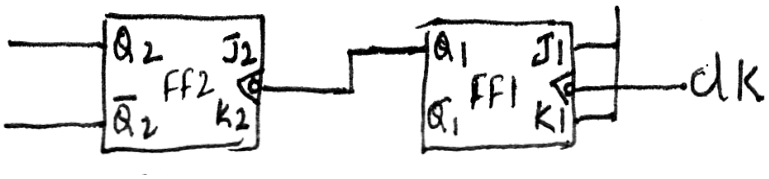
CO3: Design memory circuits.

CO4: Design shift registers and counters using flip-flops.

CO5: Derive state machine models for sequential circuits and write VHDL code for all logic circuits.

Note: ***I) PART - A*** *is compulsory.* ***Two*** *marks for each question.*

II) PART - B*: Answer any* ***Two*** *sub questions (from a, b, c) for a Maximum of* ***18 marks*** *from each unit.*

Q. No.	Questions	Marks	BLs	COs	POs
	I : PART - A	**10**			
I a.	Find the duality of the expression: $\left(AD' + B\left(C' + A\right)\right)$.	2	L1	CO1	PO1
b.	Realize, exclusive NOR using 4:1 multiplexer.	2	L1	CO2	PO1
c.	Give any two differences between PAL and PLA.	2	L2	CO3	PO1
d.	What type of counter is shown in below figure? Which flip flop is LSB? 	2	L3	CO4	PO2
e.	Define Melay model. In Moore Models output are the functions of only, i) Present State of FF ii) Input state iii) Next state iv) Both i and ii	2	L1	CO5	PO2
	II : PART - B	**90**			
	UNIT - I	**18**			
1 a.	Simplify the following expression using Boolean laws and write the logic circuit for the given expression using only NAND gate $\left(x + y'z\right) + \left(x + y'z\right)'$.	9	L3	CO1	PO1
b.	Using Quine-McClusky method find minimized SOP expression for, $F(A, B, C) = \Sigma m\,(0, 1, 5, 7)$. Draw the logic circuit for the simplified expression.	9	L3	CO1	PO3
c.	Design a combinational circuit which has four inputs *ABCD* and three outputs *wxy*. *wxy* represents the number of 1's at the input. Obtain the expressions for *wxy* using MEV method.	9	L3	CO1	PO3

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	UNIT - II	**18**			
2 a.	Design BCD to seven segment display decoder.	10	L3	CO2	PO3
b.	Implement full adder and full subtractor using demultiplexer.	8	L2	CO2	PO3
c.	Design priority encoder with inputs as I_3, I_2, I_1, I_0 and I_0 is LSB having highest priority.	8	L3	CO2	PO3
	UNIT - III	**18**			
3 a.	Implement the following function using PROM: $F_1(A, B, C) = \Sigma m(0, 1, 2, 4)$ $F_2(A, B, C) = \Sigma m(0, 5, 6, 7)$	9	L2	CO3	PO3
b.	Explain the working of D flip flop and JK flip flop with state diagram, characteristic equation and excitation table.	9	L2	CO3	PO1
c.	List the steps to convert given flip flop to another flip flop. Convert JK flip flop to D flip flop.	9	L3	CO3	PO1
	UNIT - IV	**18**			
4 a.	Define shift register. Explain with figure 4-bit serial in serial out shift register.	9	L3	CO4	PO1
b.	Explain the working of asynchronous up counter using JK FF.	9	L3	CO4	PO2
c.	Design 3-bit synchronous counter to count the sequence given below with lockout state. Use D FF. $2 \rightarrow 6 \rightarrow 7 \rightarrow 1$	9	L3	CO4	PO2
	UNIT - V	**18**			
5 a.	Write VHDL code for: i) D FF ii) 8:1 MUX	9	L2	CO5	PO1
b.	Write Melay transition, state table and state graph for Serial adder. Explain the same.	9	L2	CO5	PO2
c.	Explain with an example, Row elimination method to reduce the number of states.	9	L2	CO5	PO1

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