U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; March / April - 2022

Digital Electronic Circuits

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: Ability to apply the knowledge of mathematics and science to understand the operation of logic circuits and performance parameters.

CO2: Ability to apply the simplification techniques/methods to optimize and implement the digital functions/circuits.

CO3: Ability to analyze the given logic circuit based on the knowledge of digital elements.

CO4: Ability to design a combinational and sequential logic circuit for the given requirements/specifications.

CO5: Ability to understand and design the State machines with state graphs for sequential design.

***Note**: I) **PART - A** is compulsory. **Two** marks for each question.*

*II) **PART - B**: Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.*

Q. No.	Questions	Marks	BLs	COs	POs
	I : PART - A	**10**			
I a.	Implement the expression $y = ab + cd$ using only NAND gates.	2	L4	CO1	PO1
b.	Using 4-bit parallel adder, draw the schematic of a logic circuit to obtain BCD equivalent of EXCESS-3.	2	L3	CO3	PO2
c.	Derive the characteristic equation for T-flip-flop.	2	L2	CO1	PO1
d.	A 4-bit ripple counter has 4 flip-flops A, B, C, D. The first being flip-flop A and the last being flip-flop D. The input clock frequency is 20 kHz. The output of flip-flops BCD are fed to a NAND gate whose output is fed to CLR (clear) terminals of flip-flops. Determine the frequency of output at flip-flop D.	2	L3	CO3	PO2
e.	Write the state diagram for D flip-flop.	2	L2	CO1	PO1
	II : PART - B	**90**			
	UNIT - I	**18**			
1 a.	Convert the following Boolean functions into canonical form and express as a sum of min terms and as a product of max terms respectively. i) $f_1(a,b,c,) = ab\bar{c} + \bar{b}$ ii) $f_2(x,y,z) = (xy+z)(y+xz)$	9	L3	CO1	PO1
b.	Simplify and find the minimal sums and the minimal products for the following Boolean function using Karnaugh map method $f(a, b, c, d) = \sum m(0, 1, 2, 5, 8, 15) + \sum d(6, 7, 10)$.	9	L3	CO2	PO2
c.	Find the prime implicants and essential prime implicants for the following Boolean function using Karnaugh map method $f(a, b, c, d) = \sum m(0, 1, 3, 4, 5, 9, 11, 13, 15)$. Realize the final minimal expression using basic gates.	9	L4	CO2	PO2

Contd... 2

UNIT - II **18**

2 a.	Design and implement a circuit that accepts 2 unsigned 2-bit numbers and provides 3 outputs. The inputs are A_1A_0 and B_1B_0. The outputs are A = B, A > B and A < B.	9	L4	CO4	PO3
b.	Implement the following function using 8:1 multiplexer and external gates required if any; $f(a, b, c, d) = \sum m(1, 2, 6, 7, 9, 11, 12, 14, 15)$.	9	L4	CO4	PO3
c.	Implement the following Boolean functions using 3 to 8 line decoder: $f_1(a, b, c) = \sum m(0, 1, 6, 7)$ $f_2(a, b, c) = \sum m(1, 2, 5, 7)$	9	L4	CO4	PO3

UNIT - III **18**

3 a.	Explain the following: i) SR flip-flop operation using required timing diagram ii) Race around problem and its elimination	9	L2	CO3	PO2
b.	Implement the following: i) 3-bit parallel data storage using D-flip-flops ii) Frequency division by using JK-flip-flops iii) 2-bit counting (0, 1, 2, 3) using T-flip-flops	9	L4	CO4	PO3
c.	Construct the following: i) JK flip-flops using SR-flip-flops ii) D-flip-flops using T- flip-flops	9	L5	CO4	PO3

UNIT - IV **18**

4 a.	Design and implement a synchronous counter to sequence, $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0$ using positive edge triggered T-flip-flops.	9	L5	CO4	PO3
b.	Draw the block level schematic diagram of 4-bit SISO and PISO shift register and explain their operation with timing diagram.	9	L2	CO4	PO3
c.	Draw the block diagram of memory and its environment. Describe the read and write operation with appropriate information transfer diagram.	9			

UNIT - V **18**

5 a.	Design a sequence detector using D-flip-flop to detect sequence ending with 101.	9	L5	CO3	PO2
b.	A sequential circuit has one input (X) and one output (Z). The circuit examines groups for four consecutive inputs and produces an output Z = 1, if the input sequence 0101 or 1001 occurs. The circuit resets after every four inputs. Find the Mealy state graph.	9	L5	CO5	PO1
c.	Design a sequential Mealy circuit which converts an NRZ-coded bit stream to a Manchester-coded bit stream.	9	L5	CO5	PO1

* * *