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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fifth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; February / March - 2022

Digital CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: To Apply the basic knowledge of Physics and mathematics to understand the MOS and derive different current equations of MOS circuits and delays of CMOS inverter circuits.

CO2: To Analyze the CMOS inverter circuit and BiCMOS circuits.

CO3: To Design combinational, sequential and Dynamic circuits based on CMOS inverters for the given specifications.

CO4: To Discuss various issues related to clocking, I/O and protection in MOS and VLSI Fabrication Process.

CO5: Work in groups to model transistors and its circuits learning new tools.

Note: ***I) PART - A*** *is compulsory.* ***Two*** *marks for each question.*

II) PART - B*: Answer any* ***Two*** *sub questions (from a, b, c) for Maximum of* ***18 marks*** *from each unit.*

Q. No.	Questions	Marks	BLs	COs	POs
	I : PART - A	**10**			
I a.	Define scaling.	2	L3	CO1	PO1
b.	Define noise margin and mention the types of noise margins in MOSFET.	2	L3	CO1	PO1
c.	Write CMOS circuit for NAND-3 gate.	2	L4	CO2	PO2
d.	Write the types of high performance dynamic CMOS logic circuit.	2	L3	CO1	PO1
e.	Write BiCMOS inverter circuit with resistive base pull-down.	2	L4	CO2	PO2
	II : PART - B	**90**			
	UNIT - I	**18**			
1 a.	With the help of flow chart, explain the VLSI design flow in detail, also write drain current equation in linear and saturation region of NMOS transistor.	9	L3	CO1	PO1
b.	Explain constant field scaling techniques and its effect on device performance. Also calculate the drain current and power dissipation after scaling.	9	L3	CO1	PO1
c.	Derive an equation for the threshold voltage reduction ΔV_{To} due to short channel effects in MOSFET.	9	L4	CO2	PO2
	UNIT - II	**18**			
2 a.	Consider a simple abrupt PN-junction, which is reverse biased with a voltage V_{bias}. The doping density of the *n*-type region is $N_D = 10^{19}$ cm^{-3} and the doping density of the *p*-type region is given as $N_A = 10^{16}$ cm^{-3}. The junction area is A = 20 μm x 20 μm. Find the average junction capacitance. If the applied voltage changes from 0 V to –5 V.	9	L4	CO3	PO3

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b.	Discuss the operation of CMOS inverter along with circuit diagram and VTC curve. Also, write operating regions of nMOS and pMOS transistor.	9	L3	CO2	PO2
c.	Discuss the RC delay model and Elmore's delay model for the calculation of interconnects delay.	9	L3	CO2	PO2
	UNIT - III	**18**			
3 a.	Derive an equation for threshold voltage of two input CMOS NOR gate. Also write the condition for CMOS NOR_2 threshold voltage = $\frac{V_{DD}}{2}$.	9	L3	CO1	PO1
b.	Design CMOS logic circuit for the function, $Z = \overline{A(D+E)+BC}$ and draw stick layout diagram using Euler's path.	9	L5	CO3	PO3
c.	With neat diagram, explain the operation of Bistable elements.	9	L3	CO3	PO3
	UNIT - IV	**18**			
4 a.	With neat diagram, explain the basic principles of pass transistor circuit.	9	L3	CO3	PO3
b.	Briefly explain the domino CMOS logic gate.	9	L5	CO3	PO2
c.	Explain the concept of voltage Bootstrapping.	9	L4	CO4	PO2
	UNIT - V	**18**			
5 a.	With neat diagram, explain the fabrication steps involved in the NMOS transistor on *P*-type silicon.	9	L3	CO4	PO1
b.	Briefly explain BiCMOS inverter circuit with resistive base pull down.	9	L3	CO4	PO2
c.	With neat diagram, explain the ESD protection network with example.	9	L3	CO4	PO1

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