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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fifth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; February / March - 2022

System Verilog (Technical Skills - I)

Time: 2 hrs *Max. Marks: 50*

Course Outcomes

The Students will be able to:

CO1: Understand the System Verilog language constructs.

CO2: Understand the System Verilog OOPs facilities and framework for the verification.

CO3: Develop programs by applying the System Verilog facilities and framework.

CO4: Explore and understand modern software tools to perform different operations in System Verilog.

Co5: Develop the capability to learn on your own individually and in group to explore advanced technologies in system Verilog.

***Note: All** questions are **compulsory** and each question carries **TWO** marks.*

Q. No.	Questions	Marks	BLs	COs	POs
1.	The possible values for a 4 state variable are a) any combination of 0's and 1's b) any combination of 0's and 1's or X's c) any combination of 0's and 1's or Z's d) any combination of 0's and 1's or X's or Z's	2	L2	CO1	PO2
2.	Bit and byte data types in System Verilog can take states a) 0,1,X,U b) 0,1,X,Z c) 0,1 d) 0,1,X	2	L3	CO1	PO1
3.	For dynamic arrays, memory is allocated during a) Compilation b) Simulation c) Compilation or simulation e) Pre-processing	2	L2	CO2	PO2
4.	In System Verilog struct is a a) Pack of different data types b) Pack or collection of different data types c) Collection of different data types d) Groups data fields together or collects different data types together	2	L4	CO2	PO2
5.	Elements of queue are numbered from a) 0 to number of elements b) 1 to $ c) 1 to number of elements d) 0 to $	2	L2	CO1	PO2
6.	A class defined through the typedef in System Verilog is resolved during a) Simulation b) Compilation c) Simulation and Synthesis d) Compilation and Synthesis	2	L4	CO2	PO3
7.	In System Verilog $random is a a) Data type b) System function c) System task d) Both b and c	2	L2	CO3	PO3

Contd… 2

8.	Which of the following statement is true a) Function can invoke a task b) Task can invoke function c) Function and task are interchangeable d) Both b and c	2	L2	CO3	PO2
9.	The value returned by the function function [5:0] add (input [4:0] x,y); return x + y; endfunction is a) 6 bit value b) 0 c) x d) 5 bit value	2	L2	CO3	PO3
10.	By default all procedures and routines in system Verilog are a) automatic b) static c) automatic and static d) static and automatic	2	L4	CO4	PO3
11.	A local variable in System Verilog is initialized a) During simulation b) Before the start of simulation c) At the start of simulation d) Depending on coding style	2	L4	CO3	PO2
12.	A class handle in System Verilog can have a) null b) Assigned address c) Depends on the context of declaration or assignment d) Unknown	2	L4	CO2	PO3
13.	new() function in System Verilog a) Is a Class constructor and nonblocking b) Is a Class constructor and blocking c) Has no return type d) a and c e) b and c	2	L2	CO2	PO2
14.	Objects and Handles can be copied by a) Shallow copy b) Deep copy c) Shallow and Deep copy d) None of these	2	L3	CO3	PO2
15.	$urandom in System Verilog returns a) Random integer b) Random value with specific width c) Random unsigned value within limits permitted as per declaration d) Random unsigned value	2	L2	CO3	PO3

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16. Execution of the code will display
```
module tb;
initial begin
integer s = mul(1'bx, 1'bx);
$display ("mul(3,4) =%0d", s);
end
function
integer mul (integer x, int y);
mul = x * y;
end function   end module
```
a) mul(3,4) = 12 b) mul(3,4) = 0 c) mul(3,4) = x d) mul(3,4) = z — 2 L4 CO5 PO4

17. Which of the following statement is syntactically incorrect?
a) randc rand bit [2:0] addr2; b) randc bit [2:0] addr2; c) rand bit [2:0] addr2; d) randc bit [0:2] addr2; — 2 L4 CO3 PO3

18. Immediate assertions are like
a) Sequential statements b) Procedural statements c) Blocking statements d) Concurrent statements — 2 L2 CO3 PO2

19. A class can contain
a) Function b) Task c) Task and Function d) Only function and no task — 2 L2 CO2 PO2

20. External access to the class members can be protected by
a) Declaring members as static b) Declaring members as automatic c) Declaring members as local d) Declaring members as protected — 2 L3 CO2 PO3

21. try put()
a) places the message into mail box
b) places the message into mail box with blocking
c) places the message into mail box without blocking
d) places the message into mail box with or without blocking — 2 L4 CO3 PO3

22. In system Verilog, an event
a) Synchronizes threads b) Controls semaphores c) Controls message flow d) a, b and c e) b and c — 2 L3 CO2 PO2

23. In System Verilog semaphore
a) Provides controlled access to resources
b) Controls the resource allocation
c) a and b d) Provides restricted access to users — 2 L2 CO3 PO3

24. In system Verilog, an event
a) can be assigned to null b) can be assigned to other event variables c) can be passed to routines d) all of the above — 2 L3 CO3 PO3

25. In System Verilog Coverage is point can be
a) integral variable b) integral expression c) a or b d) logic type — 2 L2 CO3 PO1

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