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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Electrical and Electronics Engineering

Semester End Examination; March / April - 2022

Digital Electronics Circuits

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: To analyze the different switching algebra theorems and apply them for logic functions.

CO2: Explain and analyze the Karnaugh map for a few variables & combinational circuits: half adders / subtractors, encoders / decoders.

CO3: Explain and analyze the bistable element and the different latches and flip flops.

CO4: Explain and analyze sequential circuits, like counters and shift registers.

CO5: Explain and analyze the concepts of A/D and D/A converters.

Note: ***I) PART - A*** *is compulsory.* ***Two*** *marks for each question.*

II) PART - B*: Answer any* ***Two*** *sub questions (from a, b, c) for Maximum of* ***18 marks*** *from each unit.*

Q. No.		Questions	Marks	BLs	COs	POs
		I : PART - A	**10**			
I	a.	Mention canonical form of Boolean equation with an example.	2	L1,2	CO1	PO1,2
	b.	Explain Duality theorem.	2	L1,2	CO1	PO1,2
	c.	What is Priority Encoder?	2	L1,2	CO2	PO1,2
	d.	Give the logic diagram of, i) SR latch and ii) Gated D latch.	2	L1,2	CO3	PO1,2
	e.	Mention the basic types of shift register in terms of data movement.	2	L1,2	CO4	PO1,2
		II : PART - B	**90**			
		UNIT - I	**18**			
1	a.	Design a three input, one output combinational circuit, which has an output to '1' when majority of input's are logic 1 and has an output equal to '0' when majority of its inputs are at logic 0.	9	L1,2,3	CO1	PO1,2
	b.	For the Boolean function $F = ab + \bar{a}b + \bar{a}c$, i) Implement it using basic gates ii) Implement using NAND only	9	L1,2,3	CO1	PO1,2
	c.	Express the following functions as mentioned: i) $\bar{a}b + bc$ in standard SOP form ii) $W.(W + X + Y)$ in standard POS form	9	L1,2	CO1	PO1,2
		UNIT - II	**18**			
2	a.	Minimize the following expression in SOP form using *K*-Map i) $f(a, b, c, d) = \sum m(0, 1, 4, 8, 9, 10) + d(2, 11)$ ii) $f(a, b, c, d) = \sum m(1, 2, 3, 5, 6, 7, 11, 12, 13, 14, 15)$	9	L1,2,3	CO2	PO1,2
	b.	Minimize the expression using Quine Mccluskey method, $Y = \bar{A}B\ \bar{C}\ \bar{D} + \bar{A}B\ \bar{C}D + AB\ \bar{C}\ \bar{D} + AB\ \bar{C}D + A\ \bar{B}\ \bar{C}D + \bar{A}\ \bar{B}C\ \bar{D}$	9	L1,2,3	CO2	PO1,2

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	c. Write a note on look ahead carry adder with a help of Boolean function and logic diagram.	9	L1,2	CO2	PO1,2
	UNIT - III	**18**			
3 a.	Design the following function using 3 to 8 decoders: $f_1(a, b, c, d) = \sum(0, 4, 8, 10, 14, 15)$ and $f_2(a, b, c, d) = \sum(3, 7, 9, 13)$	9	L1,2,3	CO2	PO1,2,12
	b. Design Octal to Binary Encoder.	9	L1,2,3	CO3	PO1,2,12
	c. Convert SR flip flop to JK flip flop.	9	L1,2,3	CO3	PO1,2,12
	UNIT - IV	**18**			
4 a.	A sequential circuit with two D-flip flop A and B and input X and output Y is specified by the following next state and output equation, $A(t+1) = AX + BX$, $B(t+1) = \bar{A}\bar{X}$, $Y = (A+B)\bar{X}$. Derive the state diagram.	9	L3	L1,2,3	PO1,2,3,12
	b. Design a synchronous decade counter using D-flip flop.	9	L3	L1,2,3	PO1,2,3,12
	c. Explain shift left serial in serial out shift register.	9	L4	L1,2,3	PO1,2,10,12
	UNIT - V	**18**			
5 a.	Explain successive approximation ADC with neat diagram.	9	L1,2,3	CO5	PO1,2,3,12
	b. With the help of a neat diagram, explain the working of R-2R ladder network.	9	L1,2,3,4	CO5	PO1,2,3,12
	c. Explain with logic circuit, two input NAND gate CMOS circuit.	9	L1,2,3	CO5	PO1,2,3,12

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