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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Information Science and Engineering

Semester End Examination; March / April - 2022

Digital Design

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: Apply the principles of Boolean algebra/K - Map to manipulate and minimize logic expressions/functions.

CO2: Analyze and design Arithmetic Circuits and Data processing Circuits.

CO3: Design different units that are elements of typical computer's CPU using VHDL.

CO4: Design logic circuits using flip-flops/latches/registers.

CO5: Analyze and design Asynchronous and Synchronous Sequential circuits.

***Note**: I) **PART - A** is compulsory. **Two** marks for each question.*

*II) **PART - B**: Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.*

Q. No.		Questions	Marks	BLs	COs	POs
		I : PART - A	**10**			
I	a.	Draw the logic circuit for the Boolean expression $Y = AB' + A'B$.	2	L1	CO1	PO1
	b.	Draw the truth table for 2:4 decoder.	2	L1	CO2	PO1
	c.	Write the excitation table of JK flip flop.	2	L1	CO3	PO1
	d.	Write the truth table of 4-bit Johnson counter	2	L1	CO4	PO1
	e.	Write the state diagram of D flip flop.	2	L1	CO5	PO1
		II : PART - B	**90**			
		UNIT - I	**18**			
1	a.	Perform the following operations (show the step by step calculation) i) $(0.8125)_{10} = (\ )_2$ ii) $(29.45)_{10} = (\ )_8$ iii) $(0.A38)_{16} = (\ )_2$	9	L3	CO1	PO1
	b.	i) Draw the AND, OR, NOT gates using NAND gates. ii) Simplify the expression using *K*-Map method, $F = (A, B, C, D) = \sum m(3, 5, 12, 13) + d(7, 8, 10, 11)$	9	L3	CO1	PO1
	c.	Write the truth table and logic circuits for the following Boolean expression: i) F = (A+B) + C ii) F = (A+B).C′ iii) F = AB′ + AC iv) F = (A′+B) (A+B′) v) F = (A+B)′.C	9	L3	CO1	PO2
		UNIT - II	**18**			
2	a.	Simplify the following function using Quine-Mecclusky method, $F(A, B, C, D) = \sum(2, 6, 8, 9, 10, 11, 14, 15)$.	9	L3	CO2	PO2
	b.	Define decoders. Explain 2:4 decoder using logic gates and design a Full adder circuit using decoder IC.	9	L2	CO2	PO1

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	c.	Define Multiplexer. Explain 4 to 1 multiplexer with neat circuit diagram. Implement Boolean function $F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$ using multiplexer.	9	L2	CO2 PO1
		UNIT - III	**18**		
3	a.	Explain a 4-bit carry look-ahead adder.	9	L2	CO3 PO1
	b.	Explain clocked SR flip flop and JK flip flop with neat circuit diagram and timing diagram.	9	L2	CO3 PO1
	c.	Derive the characteristic equation, draw state transition diagram and excitation table of the D and T flip flops. Implement SR flip flop using JK flip flop.	9	L2	CO3 PO1
		UNIT - IV	**18**		
4	a.	Explain ring counter and johnson counter in detail.	9	L1	CO4 PO1
	b.	Design an asynchronous decade counter and explain with timing diagram.	9	L2	CO4 PO1
	c.	Design mod-5 synchronous counter using JK flip flop and implement the same.	9	L2	CO4 PO1
		UNIT - V	**18**		
5	a.	Design a simple detector circuit for the sequence 011 using Moore model.	9	L2	CO5 PO1
	b.	Reduce state transition diagram (Moore model) of Fig. 5(b) by row elimination method and implication table method.	9	L2	CO5 PO1

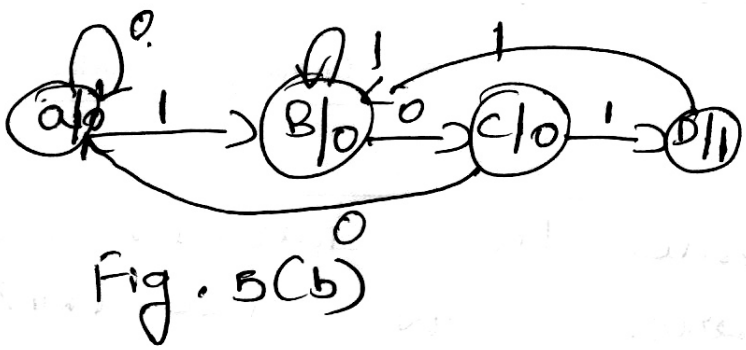

Fig. 5(b)

	c.	Analyse the Melay model asynchronous sequential circuit of Fig. 5(c) and show its stable state and corresponding outputs and also give the state diagram of this circuit.	9	L3	CO5 PO1

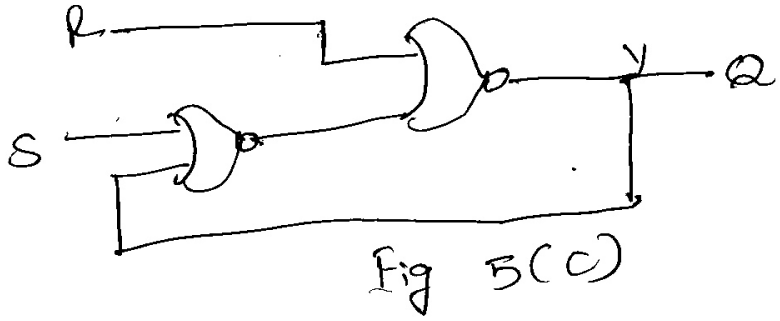

Fig 5(c)

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