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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Information Science and Engineering
Semester End Examination; March / April - 2022
Computer Organization and Architecture

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:
CO1: Analyze program execution.
CO2: Explain the basic input/output operations.
CO3: Develop the control sequence for a given instruction.
CO4: Design the memory system using various techniques.
CO5: Analyze different algorithms for performing arithmetic operations and understand need for multithread.

***Note:** **I) PART - A** is compulsory. **Two** marks for each question.*
***II) PART - B**: Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.*

Q. No.	Questions	Marks	BLs	COs
	I : PART - A	**10**		
I a.	Write basic performance equation and explain each term.	2	L2	CO1
b.	List operations performed by call and branch instructions.	2	L1	CO2
c.	Write actions required to perform read operation for the instruction, *MOV* (R_1), R_2	2	L2	CO3
d.	Differentiate SRAM and DRAM.	2	L2	CO4
e.	Write Amdahl's law equation.	2	L2	CO5
	II : PART - B	**90**		
	UNIT - I	**18**		
1 a.	Explain connection between processor and memory which is established during instruction execution.	9	L2	CO1
b.	With an example, list and explain basic instruction types.	9	L2	CO1
c.	Explain different types of addressing modes.	9	L2	CO1
	UNIT - II	**18**		
2 a.	Explain Basic push, pop operation, push and pop using auto increment and auto decrement, Routine used for safe push and safe pop operation with respect to stack.	9	L2	CO2
b.	What are interrupts? Discuss different approaches used by the processor to handle simultaneous requests.	9	L2	CO2
c.	Discuss input and output operation of asynchronous bus.	9	L2	CO2
	UNIT - III	**18**		
3 a.	Explain Multi bus organization of a processor.	9	L2	CO3
b.	Write a control sequence for *ADD* (*R3*), *R1* and unconditional branch instruction.	9	L3	CO3
c.	Discuss concept of fetching a word from a memory.	9	L2	CO3

		Marks	Level	CO
	UNIT - IV	**18**		
4 a.	Explain direct and associative cache mapping.	9	L2	CO4
b.	Explain static RAM cell and CMOS memory cell.	9	L2	CO4
c.	Explain with neat representation the memory hierarchy based on speed, size and cost.	9	L2	CO4
	UNIT - V	**18**		
5 a.	Perform sequential multiplication of $M = 1101$ and $Q = 1011$ and also write circuit for binary multiplier.	9	L3	CO5
b.	Explain Flynn's taxonomy.	9	L2	CO5
c.	Discuss multi threading on single-core versus multi-core platform.	9	L2	CO5

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