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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; June- 2022

CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

Course Outcome

The Students will be able to:

CO1: To acquire the knowledge of MOSFETs Characteristics, Fabrication Process, Combinational, sequential, dynamic circuits, Semiconductor Memories.

CO2: To Discuss the Techniques to estimate the delay and Power in MOSFETs.

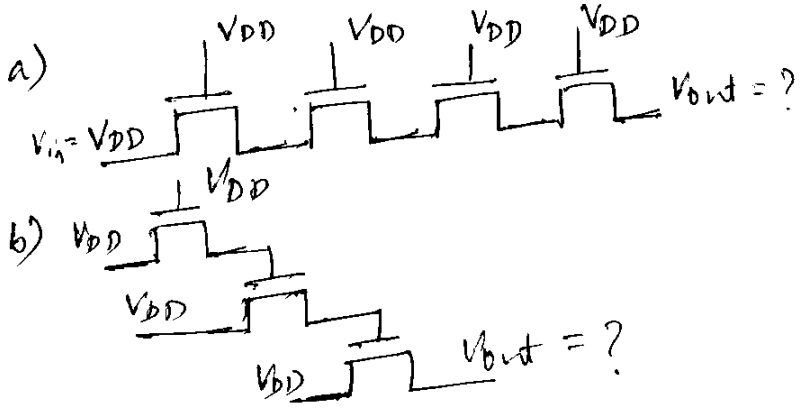
CO3: To design combinational, sequential and Dynamic logic circuits based on CMOS for the given specifications.

CO4: To Analyse the issues, challenges, models, methodologies in CMOS Fabrication Process.

Note: I) *Answer any **FIVE** full questions, selecting **ONE** full question from each unit.*

II) *Any **THREE** units will have internal choice and remaining **TWO** unit questions are compulsory.*

III) *Each unit carries 20 marks.*

Q. No.	Questions	Marks	BLs	COs	POs
	UNIT - I	**20**			
1 a.	Explain the CMOS inverter transfer characterization. Highlighting the regions of operation of the MOS transistor.	10	L2	CO1	PO2
b.	Explain the following: Non-ideal effect channel length modulation and body effect.	6	L2	CO1	PO2
c.	Find output voltage in each case as shown below: Assume $V_{DD} = 5$ V, $V_{TO} = 1$V, neglect body bias effect 	4	L1	CO1	PO2
	OR				
1 d.	With necessary diagram, explain photolithography process in CMOS Fabrication.	8	L2	CO1	PO2
e.	Explain in detail about layout design rules.	8	L2	CO1	PO3
f.	Mention any two differences between MOSIS based (λ-based) and micron design rules.	4	L1	CO1	PO2

Contd…2

	UNIT - II	**20**			
2 a.	Explain manufacturing issues in MOSFET.	10	L2	CO2	PO3
b.	Develop the RC delay model to compute the delay of the logic circuit and calculate the delay of unit sized inverter driving another unit inverter.	10	L3	CO2	PO2
	OR				
2 c.	Explain linear delay model. Compare the logical efforts of the following gates with the help of schematic diagram: i) 2-input NAND gate ii) 3-input NOR gate iii) Unit sized inverter	10	L2	CO2	PO2
d.	Discuss sources of power dissipation in CMOS circuits.	10	L3	CO2	PO2
	UNIT - III	**20**			
3 a.	What is a spice simulation model? Discuss effect of gate capacitance and parasitic capacitance during estimating gate delay.	8	L1	CO3	PO3
b.	Explain Cascode Voltage Switch Logic (CVSL). Realize 2-input AND/NAND using CVSL.	6	L2	CO3	PO3
c.	Illustrate the cascading problem in a dynamic CMOS logic. How is it overcome?	6	L2	CO3	PO3
	UNIT - IV	**20**			
4 a.	Discuss conventional circuit design of CMOS latches and CMOS flip flops with example.	8	L2	CO3	PO2
b.	Explain basic principle of pass transistor circuit with necessary circuit diagram.	8	L2	CO3	PO2
c.	What is voltage bootstrapping? Draw the circuit diagram of dynamic bootstrapping.	4	L1	CO3	PO3
	UNIT - V	**20**			
5 a.	What is the latch up problem that arises in bulk CMOS technology? Give any five guidelines for avoiding latch up.	12	L1	CO4	PO3
b.	Explain ESD protection with different models for ESD testing.	8	L2	CO4	PO3
	OR				
5 c.	Discuss the 3T DRAM cell with read and write operation.	10	L2	CO3	PO2
d.	Explain memory structures SARM with read and write circuitry with and of read and write timing diagram.	10	L2	CO2	PO2

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