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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; June - 2022

Physical Design

Time: 3 hrs

Max. Marks: 100

Course Outcome

The Students will be able to:

CO1: To apply the knowledge of graph theory in VLSI Physical Design.

CO2: To be able to analyze the VLSI Physical Design algorithms.

CO3: To be able to apply the VLSI Physical Design algorithms.

CO4: To be able to analyze the Physical Design for specific constraints.

Note: I) Answer any FIVE full questions, selecting ONE full question from each unit.

II) Any THREE units will have internal choice and remaining TWO unit questions are compulsory.

III) Each unit carries 20 marks.

IV) Missing data, if any, may suitably be assumed.

Q. No.	Questions	Marks	BLs	COs	POs
UNIT - I		20			
1 a.	Discuss Graph Theory terminology.	10	L2	CO1	PO3
b.	Given the initial partition of nodes (a-h) as shown in Fig. 1(b) can be optimally partitioned using KL algorithm, perform the first pass of the algorithm.	10	L4	CO3	PO1
<p style="text-align: center;">Figure 1(b)</p>					
UNIT - II		20			
2 a.	Illustrate the pin assignment along with example in chip planning.	10	L2	CO2	PO2
b.	Given the floor plan with blocks a-e as shown in Fig. 2(b). Generate the corresponding horizontal and vertical constraint graph. Also generate the corresponding sequence pair.	10	L4	CO2	PO5
<p style="text-align: center;">Fig. 2(b)</p>					
UNIT - III		20			
3 a.	Discuss the optimization objectives in global and detailed placement.	10	L4	CO2	PO5
b.	Perform min-cut placement to place gates a-g on a 2x4 grid as shown in Fig. 3(b), use Kernighan-Lin algorithm for partitioning. Use alternating cutline's. The cutline cut represent the initial vertical cut. Each edge on grid as capacity $\sigma_p(e) = 2$. Estimate whether the placement is routable.	10	L2	CO3	PO1

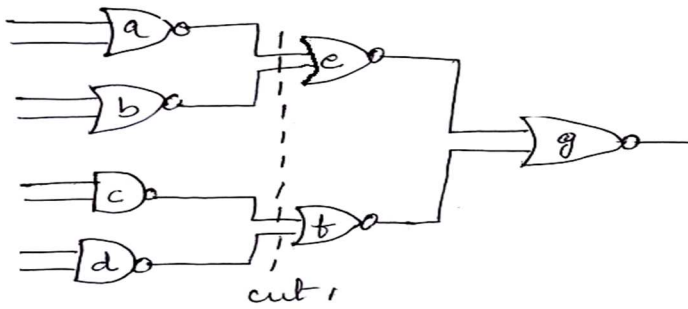
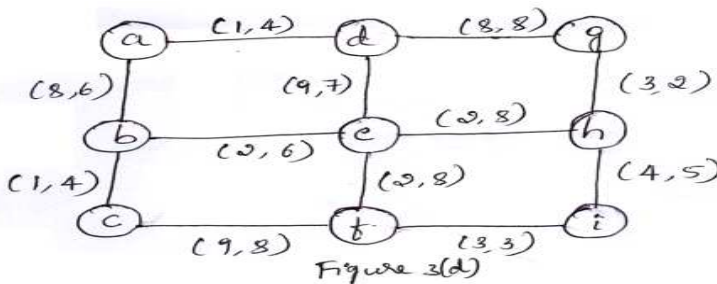


Fig. 3(b)

OR

- 3 c. Along with algorithm, explain the routing by integer linear programming. 10 L2 CO3 PO1
- d. For the graph with nine nodes (a-i) and add weights (W1, W2) as shown in Fig. 3(d). Use Dijkstra's algorithm to find the shortest path from the source S (node a) to target T (node h). Generate tables from group 2 and 3.



10 L2 CO3 PO1

UNIT - IV

20

- 4 a. Explain clocking scheme in clock routing. 08 L2 CO3 PO1
- b. Illustrate geometric matching based algorithm. 06 L4 CO2 PO5
- c. Illustrate MMM algorithm. 06 L4 CO2 PO5

OR

- d. Illustrate DME algorithm in clock routing. 10 L4 CO2 PO5
- e. Illustrate H- tree based algorithm. 10 L4 CO2 PO5

UNIT - V

20

- 5 a. Illustrate static timing analysis with example. 10 L2 CO5 PO1
- b. Illustrate delay budgeting with zero slack algorithms. 10 L4 CO4 PO5

OR

- c. Briefly explain netlist restructuring in physical synthesis. 10 L2 CO4 PO5
- d. Illustrate performance-driven design flow in timing closure. 10 L4 CO5 PO3

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