U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; June -2022

Digital system Design Using Verilog

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: To gain knowledge of Verilog modelling in term of digital system and Embedded systems.

CO2: To obtain insight to design challenges, techniques, methodology, performance criteria and design flow.

CO3: To be able to design and develop Verilog model of digital logic circuits and simple Embedded systems applications prepare and present a report.

CO4: To be able analyze synthesis report of digital logic circuits and come up with optimized design through self learning and research.

Note: I) *Answer any* ***FIVE*** *full questions, selecting* ***ONE*** *full question from each unit.*

II) *Any* ***THREE*** *units will have internal choice and remaining* ***TWO*** *unit questions are compulsory.*

III) *Each unit carries 20 marks.* ***IV)*** *Missing data, if any, may suitably be assumed.*

Q. No.	Questions	Marks	BLs	COs	POs
	UNIT - I	**20**			
1 a.	Explain functional verification and timing verification with examples.	4	L2	CO1	PO5
b.	Describe the simple design methodology starting from the requirement to testing.	6	L2	CO1	PO5
c.	Develop a test bench model for the light-controller and enable module for traffic light control. Verify the conditions that, when the enable input is 1, the output is same as the light input and when the enable input is 0, all light output are inactive.	10	L3	CO1	PO5
	UNIT - II	**20**			
2a.	Develop a verification test bench for the adder/subtractor that compares the result with the result of addition or subtraction performed on value of type integer.	8	L4	CO2	PO5
b.	Develop a datapath to perform a complex multiplication of two complex numbers. Develop a Verilog model for the same.	12	L4	CO2	PO5
	UNIT - III	**20**			
3a.	Explain the difference between asynchronous and synchronous static RAM.	6	L2	CO2	PO5
b.	Design a FIFO to store up to 256 data items of 16-bits each using a 256×16 bit dual port SSRAM for the data storage. The FIFO should provide status outputs to indicate the when FIFO is empty and full.	10	L3	CO2	PO5
c.	Discuss the purpose of logic blocks and I/O blocks in a FPGA.	4	L2	CO2	PO5

OR

Contd… 2

3 d.	Design 7-segment decoder with blanking input where blank overrides the BCD input and causes all segments not to be it using a ROM. Develop a Verilog model for the same.	10	L3	CO2	PO3
e.	Explain the photolithographic etching process in IC manufacture.	6	L2	CO2	PO3
f.	What distinguishes surface mount IC packages from insertion type packages?	4	L2	CO2	PO3
	UNIT - IV	**20**			
4 a.	Explain the Y chart representation of Verilog constructs for three views of a circuit.	5	L3	CO3	PO1
b.	Describe high level synthesis with example.	5	L3	CO3	PO1
c.	Develop, verify and synthesize BCD to Excess-3 code converter.	10	L4	CO3	PO5
	OR				
4 d.	Develop and synthesize Verilog module for a 4-bit parallel load data register.	10	L3,4	CO3	PO2,3
e.	Explain the block diagram of general organization of logic synthesis tool.	10	L2,4	CO3	PO3,5
	UNIT - V	**20**			
5 a.	With a neat diagram explain the architecture of RISC-SPM.	10	L3	CO4	PO5
b.	Explain the ASMD chart for the state machine controller of the UART transmitter.	10	L3	CO4	PO5
	OR				
5 c.	Explain the partitioned sequence machine.	10	L2	CO2,3	PO3,5
d.	Explain UART with block diagram.	10	L2	CO2,3	PO3,5

* * *