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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; June -2022

ASIC Design

Time: 3 hrs *Max. Marks: 100*

Course Outcome

The Students will be able to:

CO1: Select the type of design flow for any given system.

CO2: Design systems using cell libraries.

CO3: Develop systems with Hierarchical design flow.

CO4: Estimate the various parameters of an ASIC.

Note: I) *Answer any* ***FIVE*** *full questions, selecting* ***ONE*** *full question from each unit.*

II) *Any* ***THREE*** *units will have internal choice and remaining* ***TWO*** *unit questions are compulsory.*

III) *Each unit carries 20 marks.* ***IV)*** *Missing data, if any, may suitably be assumed.*

Q. No.	Questions	Marks	BLs	COs	POs
	UNIT - I	**20**			
1 a.	Discuss the different types of ASICs.	10	L2	CO1	PO3
b.	Discuss the functions of each step in the ASIC design flow.	5	L 2	CO1	PO3
c.	Mention important features of PLDs	5	L 1	CO 2	PO2
	OR				
1 d.	Discuss the standard cell based ASICs.	8	L 1	CO 2	PO3
e.	What are the essential characteristics of FGPA and discuss its along with the structure.	6	L 1	CO 2	PO3
f.	Discuss Gate array based ASICs.	6	L 2	CO 1	PO3
	UNIT - II	**20**			
2 a.	Mention advantages and disadvantages of datapath layout.	5	L1	CO2	PO2
b.	Discuss ripple carry adder.	8	L1	CO2	PO3
c.	Define logical effort, electrical effort and predicting delay.	7	L2	CO2	PO3
	OR				
2 d.	With the help of neat figure, discuss datapath symbol for an adder.	6	L1	CO2	PO3
e.	Derive an expression for optimum delay of the logic cell.	8	L3	CO4	PO5
f.	Write a short note on I/O cells.	6	L1	CO1	PO3
	UNIT - III	**20**			
3 a.	What is netlist screener? List the errors that can be detected by netlist screener.	10	L1	CO1	PO3
b.	Explain the following terms: i) Edit- in- place ii) Attributes iii) Back-Annotation	10	L2	CO2	PO3

Contd… 2

	UNIT - IV	**20**			
4 a.	What is EDIF? Give hierarchical nature of an EDIF file. Also explain about EDIF schematic icon.	10	L2	CO1	PO3
b.	Explain the following low-level design languages: i) ABEL ii) CUPL iii) PALASM	10	L2	CO2	PO2
	UNIT - V	**20**			
5 a.	Discuss the placement algorithms.	6	L2	CO2	PO2
b.	Write a short note on system partitioning.	6	L2	CO3	PO2
c.	Mention the goals and objectives of CAD tools.	8	L3	CO1	PO2
	OR				
5 d.	Discuss the physical design flow with neat flow diagram.	6	L3	CO2	PO3
e.	Discuss the goals and objectives of global routing.	6	L3	CO2	PO3
f.	Explain the iterative placement improvement.	8	L3	CO1	PO2

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