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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; July / Aug. - 2022

VLSI Testing and Verification

Time: 3 hrs *Max. Marks: 100*

Course Outcome

The Students will be able to:

CO1: Apply the knowledge of Digital and Analog VLSI circuits to understand the concepts of VLSI Circuit testing.
CO2: Analyze the various concepts of test generation for combinational, sequential logic circuits and BIST.
CO3: Design the testable combinational, sequential logic circuits and BIST for the given specifications.
CO4: Discuss the verification tools and verification languages.
CO5: Analyze the role of Stimulus and Response in verification.

***Note**: I) **PART - A** is compulsory. **Two** marks for each question.*
*II) **PART - B**: Answer any **Two** sub questions (from a, b, c) for a Maximum of **18 marks** from each unit.*

Q. No.	Questions	Marks	BLs	COs	POs
	I : PART - A	**10**			
I a.	What is stuck at fault techniques in VLSI testing and explain in brief.	2	L2	CO1	PO1
b.	What is reed Muller expression technique and list one drawback of the reed Muller expression technique.	2	L2	CO2	PO2
c.	List any two advantages of LSSD techniques.	2	L2	CO3	PO3
d.	Elaborate various challenges of verification in VLSI design.	2	L1	CO4	PO2
e.	What is complex response in VLSI verification?	2	L1	CO5	PO2
	II : PART - B	**90**			
	UNIT - I	**18**			
1 a.	List the bridging faults in VLSI testing and also explain with suitable example.	9	L2	CO1	PO1
b.	Explain the concept of Boolean difference in VLSI testing with suitable example.	9	L3	CO1	PO1
c.	Discuss Path-Oriented-Decision-making algorithm with the help of flow chart.	9	L3	CO1	PO1
	UNIT - II	**18**			
2 a.	Draw and explain PLA logic structure with testable three variable Boolean functions.	9	L2	CO2	PO2
b.	Explain the concept of synthesis of random pattern testable combinational circuits.	9	L2	CO2	PO2
c.	With a neat diagram explain the testing of sequential circuit as a iterative combinational circuits networks.	9	L2	CO2	PO2

	UNIT - III	**18**			
3 a.	Elaborate scan-path technique for testable sequential circuit design with suitable example.	9	L3	CO3	PO3
b.	Explain the concept of BIST with suitable example.	9	L3	CO3	PO3
c.	Write short note on:				
	i) Boundary scan	9	L3	CO3	PO3
	ii) LSSD				
	UNIT - IV	**18**			
4 a.	Explain the concept of linting and also discuss the limiting of linting tools.	9	L2	CO4	PO2
b.	What is test bench? Explain the reconvergence model in verification of VLSI design.	9	L1	CO4	PO2
c.	Discuss event based simulation and cycle based simulation and compare with co-simulation.	9	L3	CO4	PO2
	UNIT - V	**18**			
5 a.	Compare with suitable example generating a simple waveform and generating complex waveform.	9	L2	CO5	PO2
b.	Discuss the following terms:				
	i) Minimizing sampling	4	L2	CO5	PO2
	ii) Verifying the output	5			
c.	Explain the concept of self-checking test benches with suitable examples.	9	L2	CO5	PO2

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