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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; October - 2022

CMOS Mixed Mode VLSI Circuits

Time: 3 hrs *Max. Marks: 100*

Note: I) *Answer any* ***FIVE*** *full questions, selecting* ***ONE*** *full question from each unit.*

II) *Any* ***THREE*** *units will have internal choice and remaining* ***TWO*** *unit questions are compulsory.*

III) *Each unit carries 20 marks.*

Q. No.	Questions	Marks	BLs	COs	POs
	UNIT - I	**20**			
1 a.	Applying the spatial integration and the concept of potential gradient derive an expression for MOSFET'S drain current in saturation / strong inversion region.	10	L3	CO1	PO5
b.	Comment on the impact of MOSFET'S scaling in terms of effects and advantages.	5	L2	CO1	PO5
c.	Employing appropriate model's, analyze the impact of flicker and thermal noise in MOSFET'S.	5	L3	CO1	PO5
	UNIT - II	**20**			
2 a.	Draw the small signal equivalent circuit of the current mirror shown in Fig. Q2(a) and obtain expression for its output resistance.	10	L3	CO2	PO5

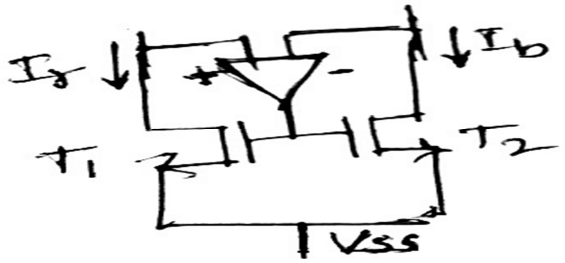
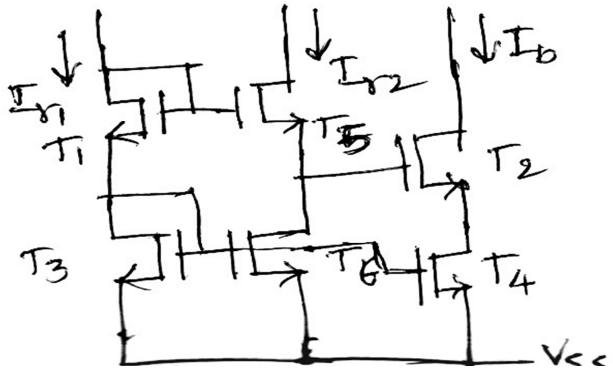


Fig. Q2(a)

b.	For the current mirror shown in Fig. Q2(b). Applying KVL find the minimum voltage to be maintained at input and output for proper mirroring operation.	10	L3	CO2	PO3



OR

2 d. Analyze the current mirror shown in Fig. Q2(d) and find its output resistance. 10 L3 CO2 PO5

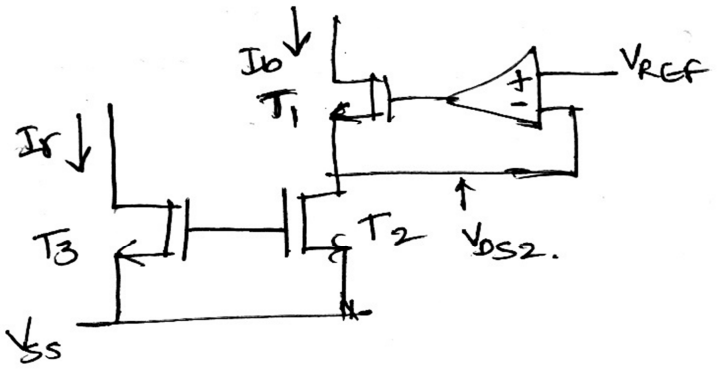


Fig. Q2(d)

e. For the circuit shown in Fig. Q2(e) the expression for V_{REF} while accounting the relation between R_4 and R_1, R_1 and R_2 for $V_{REF} = R_3 \frac{V_{Go}}{R_1}$ 10 L3 CO2 PO5

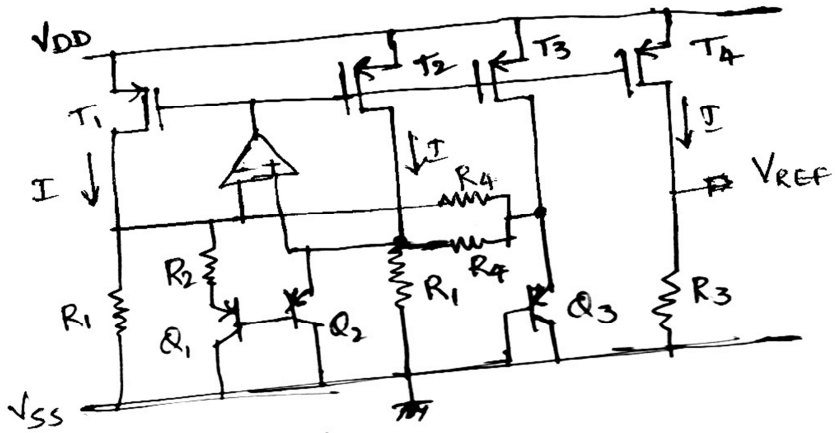


Fig. Q2(e)

UNIT - III **20**

3 a. Draw the schematic of a gain enhancing cascode amplifier along with its small signal equivalent model and show how cascoding with feedback amplifier increases output resistance. 10 L3 CO2 PO3

b. For the common source gain stage with diode connected load show that

$A_v = -\sqrt{\frac{W_1/L_1}{W_2/L_2}}$ 10 L3 CO2 PO3

OR

3 d. Draw the MOSFET level schematic of 2 stage amplifier (1st stage differential amplifier) with compensation resistance (transistor), also draw its small signal equivalent model while obtaining expression for its transfer function by employing pole-zero analysis. 10 L3 CO2 PO3

e. Comment on the amplifier characterization parameters. 10 L3 CO2 PO3

UNIT - IV **20**

4 a.	Present a qualitative view of switch error sources while analyzing the significance of contributing parameters.	10	L3	CO3	PO5
b.	For a sample and hold circuit shown that $\|H_{id}(j\omega)\| = \frac{2\pi}{\omega_S}\left\|\frac{\sin(\pi\omega/\omega_s)}{\pi\omega/\omega_s}\right\|$. Also plot its magnitude response.	10	L3	CO3	PO5

OR

4 d.	For the SC of integrator shown in Fig. Q4(d), obtain the transfer function.	10	L3	CO3	PO3

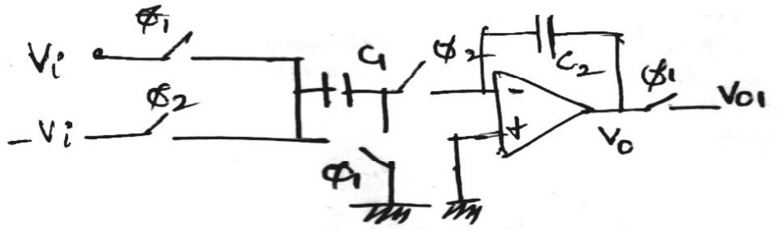


Fig. Q4(d)

e.	Draw the signal flow graph of a SC filter shown in Fig. Q4(e) and derived its transfer function.	10	L3	CO3	PO5

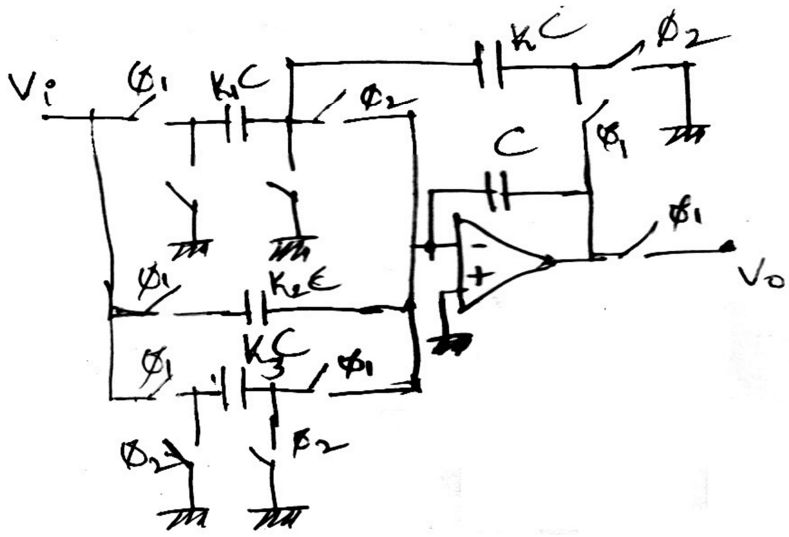


Fig. Q4(e)

UNIT - V **20**

5 a.	With required equations and plots present an analytical account of circuit component errors in converters.	10	L3	CO4	PO5
b.	Draw the block diagram of 3-bit register string DAC with a 3 to 8 decoder and illustrate its working with required table and analysis.	10	L3	CO4	PO5

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