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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M.Tech -Master in VLSI & Embedded System (MECE)

Semester End Examination; October -2022

Low Power VLSI Design

Time: 3 hrs *Max. Marks: 100*

Note: ***I)*** *Answer any* ***FIVE*** *full questions, selecting* ***ONE*** *full question from each unit.*

II) *Any* ***THREE*** *units will have internal choice and remaining* ***TWO*** *unit questions are compulsory.*

III) *Each unit carries 20 marks.*

Q. No.	Questions	Marks	BLs	COs	POs
	UNIT - I	**20**			
1 a.	Discuss various sources of power dissipation in CMOS circuits. Mention the ways to reduce old dissipation in CMOS circuits. Discuss each of them with their effects.	10	L3	CO1	PO5
b.	With suitable equations, explain sub-threshold channel leakage current of a MOS transistor.	7	L2	CO1	PO5
c.	The chip size of a CPU with in 15 mm × 25 mm clock frequency of 400 MHz operating at 2.5 V. Length of the clock routing is estimated to be twice the circumference of the chip. Assume that the clock signal is routed on metal layer with width of 1.2 μm and the parasitic capacitance of the metal layer is 1 fF/μm^2. What is the power dissipation of the clock signal?	3	L3	CO1	PO5
	OR				
1 d.	Mention the steps adopted in gate-level power simulation. What is the disadvantage with use of gate-level analysis?	6	L2	CO1	PO5
e.	What are the effects of data correlation on bit switching frequency? Explain them.	6	L3	CO1	PO5
f.	Explain in detail the steps used in the static statistical estimation of mean.	8	L2	CO1	PO5
	UNIT - II	**20**			
2 a.	Explain the propagation of a static probability in logic circuits. Also compute the transition density and static probability of the following Boolean function, if $p(a) = 0.2$, $p(b) = 0.3$, $p(c) = 0.4, D(a) = 1, D(b) = 2$ *and* $D(c) = 3$. $$y = a.b + c$$	12	L4	CO2	PO3,5
b.	Derive an expression for conditional probability and frequency under memory less random signal model. Also, compute the	8	L2	CO2	PO3,5

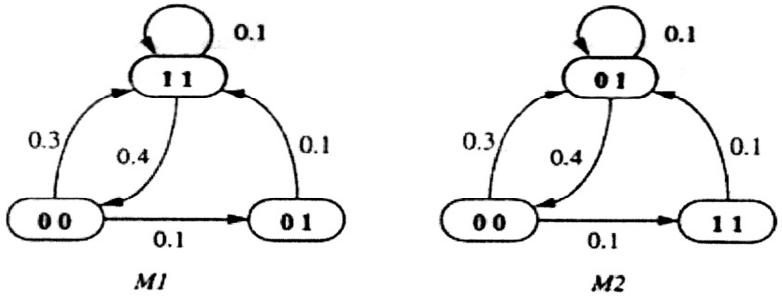
OR

2 d.	What is transistor network restructuring? Explain. Draw the four different CMOS circuit implementation for Boolean function $Y = A(B + C)$.	10	L4	CO2	PO3,5
e.	Realize positive edge-triggered D Flip-flop and analyze its working.	6	L3	CO2	PO3,5
f.	Illustrate how threshold voltage can be varied by controlling the bulk bias voltage.	4	L2	CO2	PO3,5

UNIT - III **20**

3 a.	Discuss with circuits, various local transformation operators for gate reorganization.	10	L2	CO4	PO5
b.	Draw and explain the architecture of bus invert coding. Write the equation for expected number of transaction for regular bus and inverted bus. Also listed values for $n = 4$.	10	L3	CO4	PO5

OR

3 d.	Draw and explain delay balance multiplier cell. List on application of it.	7	L2	CO3	PO3,5
e.	Explain the bit line isolation used to reduce bit line swing in a SRAM.	6	L2	CO3	PO3,5
f.	Explain transaction analysis of state and encoding. Also compute the expected state transaction for the following two machines. 	7	L4	CO3	PO3,5

UNIT - IV **20**

4 a.	With the help of a block diagram explain performance management by voltage control.	8	L2	CO4	PO5
b.	What is CDFG? Draw the CDFG of a system that computes $Y_n = a_n b_n + 5a_{n-1}$. Use this to derive system hardware architecture.	6	L4	CO4	PO5
c.	With help of a block diagram, explain asynchronous process unit.	6	L2	CO4	PO5

UNIT - V **20**

5 a.	Illustrate the following source of power dissipation in the DRAM and SRAM: i) Activate power sources ii) Data retention power sources	12	L2	CO3	PO3,5
b.	Realize 16-bit carry select adder and list its operation.	8	L3	CO3	PO3,5