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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M.Tech -Master in VLSI & Embedded System (MECE)

Semester End Examination; October -2022

ARM Processors

Time: 3 hrs *Max. Marks: 100*

Note: ***I)*** *Answer any* ***FIVE*** *full questions, selecting* ***ONE*** *full question from each unit.*

II) *Any* ***THREE*** *units will have internal choice and remaining* ***TWO*** *unit questions are compulsory.*

III) *Each unit carries 20 marks.*

Q. No.	Questions	Marks	BLs	COs	POs
	UNIT - I	**20**			
1 a.	Explain in brief the advantages of Cortex-M processors.	10	L2	CO1	PO5
b.	With a neat diagram, explain a simplified software development flow.	10	L2	CO1	PO5
	OR				
1 d.	With a neat diagram, explain briefly the software flow.	10	L2	CO1	PO5
e.	Explain briefly the block diagram of Cortex-M3 and Cortex-M4 processor.	10	L2	CO1	PO5
	UNIT - II	**20**			
2 a.	Discuss the different operation modes and states of Cortex-M3 and Cortex-M4 processors.	7	L2	CO2	PO3
b.	Explain briefly the memory system features of Cortex-M3 and Cortex-M4 processors.	7	L2	CO2	PO3
c.	Explain briefly about Nested Vectored Interrupt Controller (NVIC).	6	L2	CO2	PO3
	OR	**20**			
2 d.	Explain briefly about memory access attributes.	6	L2	CO3	PO5
e.	Explain briefly memory system in a Microcontroller.	8	L2	CO3	PO5
f.	What are the advantages of big based operations?	6	L2	CO3	PO5
	UNIT - III				
3 a.	Explain briefly exception sequence overview.	10	L2	CO2	PO3
b.	Explain in brief the details of SCB registers for exception and interrupt control.	10	L2	CO2	PO3
	OR				
3 d.	Write a note on; i) Interrupt latency ii) Interrupt at multiple cycle instruction iii) Tail chaining iv) Lazy stacking	20	L2	CO2	PO3

	UNIT - IV	**20**			
4 a.	List low power system requirements and enumerate on low power characteristics of Cortex-M3 and Cortex-M4 processors.	8	L1	CO3	PO5
b.	With a neat diagram, explain the operations of Systick timer.	8	L2	CO4	PO5
c.	Explain briefly about Memory Protection Unit (MPU).	4	L2	CO4	PO5
	UNIT - V	**20**			
5 a.	Explain briefly faults related to exception handling.	10	L2	CO4	PO5
b.	Write a note on;				
	i) Debug modes	10	L2	CO4	PO5
	ii) Debug events				

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