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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M.Tech - Master in VLSI & Embedded System (MECE)

Semester End Examination; October -2022

Design of VLSI Systems

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: Apply the knowledge the VLSI System Design Methodology, Chip Design Methods and various concepts of Design Capture Tools.

CO2: Analyze the Data Path Sub System Design and Array Subsystem Design.

CO3: Develop the memory system and special purpose Subsystems.

CO4: Design and develop VLSI System Testing and Verification.

Note: ***I)*** *Answer any* ***FIVE*** *full questions, selecting* ***ONE*** *full question from each unit.*

II) *Any* ***THREE*** *units will have internal choice and remaining* ***TWO*** *unit questions are compulsory.*

III) *Each unit carries 20 marks.*

Q. No.	Questions	Marks	BLs	COs	POs
	UNIT - I	**20**			
1 a.	Explain the term; Hierarchy, Regularity, Modularity and Locality with one example each.	10	L2	CO1	PO1
b.	Explain the gate array based design using the basic structure of gate arrays and sea of gates diagram.	10	L2	CO1	PO1
	OR				
1 d.	Discuss briefly on standard cell based design and full custom design.	10	L2	CO1	PO1
e.	With help of neat diagram, explain the generalized design flow.	10	L2	CO1	PO1
	UNIT - II	**20**			
2 a.	Define simulation. Explain the different simulation methods used in design verification tools.	10	L1	CO2	PO1
b.	Explain the following design capture tools with tool names: i) HDL Design ii) Schematic Design iii) Chip Composition	10	L2	CO1	PO1
	UNIT - III	**20**			
3 a.	Design a 16-bit carry select adder using 4-bit adder, in each group write expression for critical path delay.	10	L3	CO2	PO2
b.	Draw the schematic diagram of a comparator to compare the magnitude of two 4-bit binary number using adders. Discuss the operation for unsigned and signed comparison.	10	L3	CO2	PO2

Contd ... 2

OR

3 d.	Discuss Funnel Shifter and Barrel Shifter.	10	L2	CO2	PO2
e.	Sketch and explain pseudo-n MOS NOR ROM for the following contents: word 0:100010 word 1:001100 word 2:100101 word 3:101010	10	L2	CO2	PO2
	UNIT - IV	**20**			
4 a.	Design clock generation and clock distribution concept of clock system architecture.	10	L2	CO3	PO3
b.	Briefly explain the concept of PLL's and DLL's of clock generation.	10	L2	CO3	PO3
	OR				
4 d.	List the properties of I/O of system and explain any two basic I/O pad circuits.	10	L2	CO3	PO3
e.	Describe the basic principle of ESD protection and also basic components of the general ESD protection networks.	10	L2	CO3	PO3
	UNIT - V	**20**			
5 a.	Explain the following with respect to IC design economics: i) Non-Recurring engineering cost ii) Recurring cost iii) Fixed cost.	10	L2	CO4	PO3,4,5
b.	Explain the following with respect to design for testability: i) Adhoc testing ii) Built-In-Self-Test (BIST)	10	L2	CO4	PO3,4,5

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