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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Computer Science and Engineering

Semester End Examination; August - 2023

Computer Architecture

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: Describe the evolution of computers.

CO2: Analyze the basic properties of pipelining.

CO3: Understand the Instruction Level Parallelism and Its Exploitation.

CO4: Discuss system architecture of multiprocessor and Thread Level Parallelism.

CO5: Analyze the steps to perform parallelization of computation.

***Note**: I) **PART-A** is compulsory. **Two** marks for each question.*

*II) **PART-B**: Answer any **Two** sub questions (from a, b, c) for a Maximum of **18 marks** from each unit.*

Q. No.	Questions	Marks	BLs	COs	POs
	I : PART - A	**10**			
1 a.	Mention the different classes of computers.	2	L2	CO1	PO1,2,3
b.	What are the three classes of instructions of RISC architecture?	2	L2	CO2	PO1,2,3,4
c.	How many bits are in the (0, 2) branch predictor with 4k entries?	2	L3	CO3	PO1,2,3
d.	Differentiate between coherence and consistency.	2	L2	CO4	PO1,2,3,4
e.	What are the major performance goals of the parallelization process?	2	L2	CO5	PO1,2,3,4
	II : PART - B	**90**			
	UNIT - I	**18**			
2 a.	What is parallelism? Explain the different classes of parallelism.	9	L2	CO1	PO1,2,3
b.	Explain the different categories of operation performed on MIPS. Also summarize the MIPS ISA.	9	L2	CO1	PO1,2,3
c.	Explain the terms MTTF, MTBF and MTTR. Assume a disk subsystem with the following components and MTTF: • 10 disks, each rated at 1,000,000-hour MTTF • 1 SCSI controller, 500,000-hour MTTF • 1 power supply, 200,000-hour MTTF • 1 fan, 200,000-hour MTTF • 1 SCSI cable, 1.000.000-hour MTTF Using the simplifying assumptions that the lifetimes are exponentially distributed and those failures are independent. Compute the MTTF of the system as a whole.	9	L3	CO1	PO1,2,3

Contd…2

UNIT - II **18**

3 a.	What is pipelining? How pipelining is implemented in 5 clock cycles.	9	L2	CO2	PO1,2,3,4
b.	Consider the un-pipelined processor. Assume that it has a 1 ns clock cycle and that it uses 4 cycles for ALU operations and branches and 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose that due to clock skew and setup, pipelining the processor adds 0.2 ns of overhead to the clock, ignoring any latency impact, how much speedup in the instruction execution rate will we gain from a pipeline?	9	L3	CO2	PO1,2,3,4
c.	What is a hazard? Explain the major hurdle of pipelining.	9	L3	CO2	PO1,2,3,4

UNIT - III **18**

4 a.	Explain the terms: i) Data dependences ii) Name dependences iii) Data hazard iv) Control dependences	9	L2	CO2	PO1,2,3
b.	Explain the basic structure of MIPS floating-point using Tomasulo's algorithm with help of a diagram.	9	L2	CO2	PO1,2,3
c.	Show what the information tables look like for the following code sequence when only the first load has completed and written its result. Show the result in the form of three tables. 1. L.D F_6, 32(R_2) 2. L.D F_2, 44(R_3) 3. MUL.D F_0, F_2, F_4 4. SUB.D F_8, F_2, F_6 5. DIV.D F_{10}, F_0, F_6 6. ADD.D F_6, F_8, F_2	9	L3	CO3	PO1,2,3

UNIT - IV **18**

5 a.	Explain the basic structure of a centralized shared-memory multiprocessor based on a multicore chip with a neat diagram.	9	L2	CO4	PO1,2,3
b.	What are multiple cache coherence problems? Explain the different cache coherence protocols.	9	L2	CO4	PO1,2,3
c.	Explain the cache coherence steps and bus traffic for three processors P_0, P_1, P_2.	9	L2	CO4	PO1,2,3

UNIT - V **18**

6 a.	Explain the various steps involved in developing parallel applications with a neat diagram.	9	L2	CO5	PO1,2,3,4
b.	With pseudo code, explain the decomposition of "Equation solver kernel".	9	L2	CO5	PO1,2,3,4
c.	With pseudo code, describe the parallel equation solver with explicit message passing.	9	L2	CO5	PO2

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