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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; August - 2023

Analog CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: Apply the knowledge of physics circuit elements and circuit analyse tom understand the MOS devices and analog COMS.

CO2: The analyse different analog COMS VLSI circuits amplifiers, Op-amps, Oscillators.

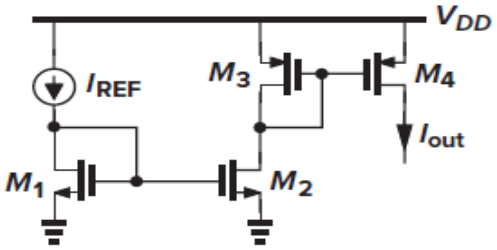
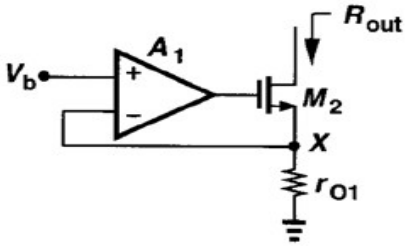
CO3: The Design the analog CMOS circuits for the given Specifications.

CO4: The Develop analog CMOS circuits for Different applications.

CO5: To Simulate the analog CMOS circuits using modern tools.

***Note**: I) **PART-A** is compulsory. **Two** marks for each question.*

*II) **PART-B**: Answer any **Two** sub questions (from a, b, c) for a Maximum of **18 marks** from each unit.*

Q. No.		Questions	Marks	BLs	COs	POs
		I : PART - A				
1	a.	Draw the small signal model of a common gate amplifier.	2	L3	CO1	PO1
	b.	Find the drain current of MOSFET M_2 in Fig. 1.b.  Fig. 1.b.	2	L3	CO2	PO2
	c.	State the condition for applicability of Miller's theorem.	2	L2	CO1	PO1
	d.	Find R_{out} in Fig. 1.d  Fig. 1.d.	2	L3	CO1	PO1
	e.	Given the transfer function of a four-stage oscillator, H(s) find the minimum voltage gain per stage to produce sustained oscillations. $$H(s) = -\frac{A_0^4}{\left(1+\frac{s}{\omega_0}\right)^4}$$	2	L3	CO2	PO2

Contd...2

		II : PART - B	**90**			
		UNIT - I	**18**			
2	a.	Find the voltage gain of the common source amplifier of Fig 2.a. with V_{DD} = 5 V, R_D = 5 kΩ, $\mu_n C_{ox}$ = 100 μA/V2, W = 50 μm, L = 1μm, V_i = 0.8 V, L_d = 0, X_d = 0, and λ = 0. Assume that the bias value of V_i is 1 V.	9	L3	CO2	PO2

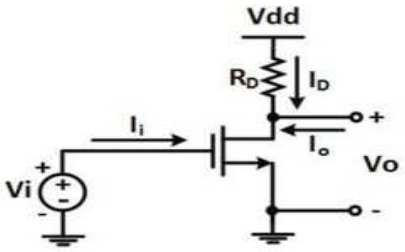


Fig. 2.a.

	b.	Draw the small signal model of Common Source Amplifier with resistive load and source degeneration resistor show that its voltage gain, $Av = -\frac{g_m R_D}{1 + g_m R_S}$	9	L3	CO2	PO2
	c.	Calculate the voltage gain of the circuit shown in Fig. 2.c. if λ = 0.	9	L4	CO2	PO2

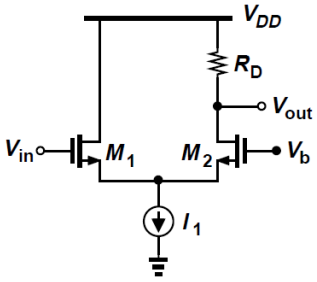


Fig. 2.c.

		UNIT - II	**18**			
3	a.	With required schematics and equations illustrate the construction and working of a Variable Gain Amplifier (VGA) or Gilbert Cell.	9	L3	CO3	PO3
	b.	Illustrate the need of cascade current mirror. For the current mirror shown in Fig 3.b find the voltage V_N and condition for the ratio of MOSFET dimensions to make I_{out} to track I_{REF} accurately.	9	L4	CO1	PO1

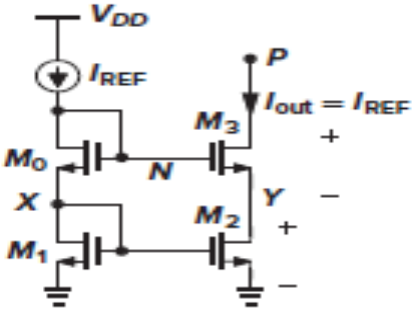


Fig. 3.b.

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c. Applying the small signal analysis obtain the expression for differential gain, A_d of the amplifier shown in Fig. 3.c.

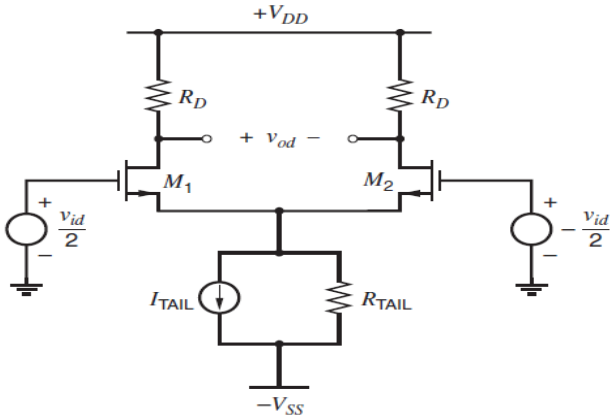

Fig. 3.c.

9 L3 CO3 PO3

UNIT - III **18**

4 a. State Miller's theorem, analyze the circuit in Fig. 4a. for applicability of Miller's theorem.

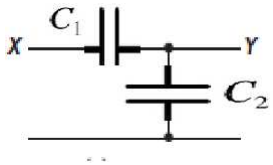

Fig. 4.a.

9 L4 CO1 PO1

b. For the Common Source stage of Fig 4.b, applying the small signal analysis obtain/derive the expression for transfer function and the poles.

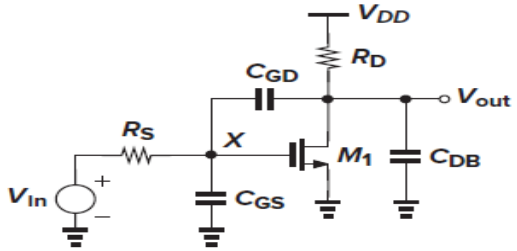

Fig. 4.b.

9 L4 CO2 PO2

c. The common gate stage of Fig. 4.c. is designed with $(W/L)_1=50/0.5$, $I_{D1}=1ma$, $R_D=2\ k\Omega$, and $R_s=1\ k\Omega$ assuming $\lambda=0$, determine the poles and low frequency gain.

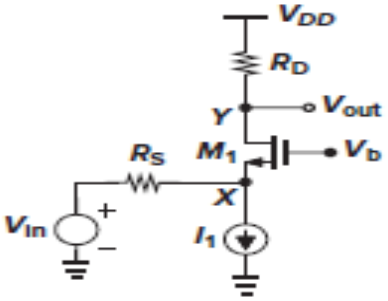

Fig. 4.c.

9 L4 CO2 PO2

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UNIT - IV **18**

5 a. Identify the topology of amplifier in Fig. 5.a. and designate the role of each MOSFET's in its working, also derive an expression for its gain. 9 L4 CO2 PO2

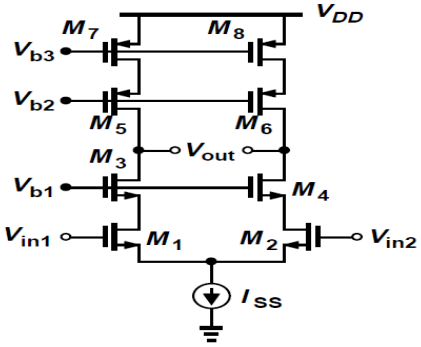

Fig. 5.a.

b. Present qualitative analysis of operational amplifier performance parameters. 9 L4 CO3 PO3

c. Calculate the low frequency PSRR of the feedback circuit shown in Fig. 5.c. 9 L3 CO2 PO2

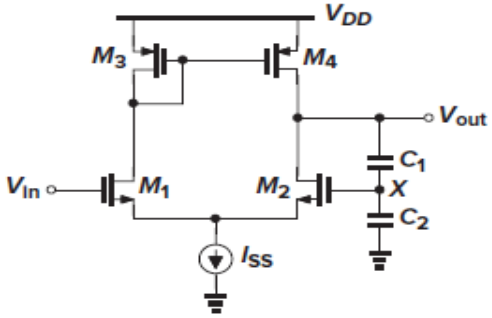

Figure 5.c.

UNIT - V **18**

6 a. Calculate the noise spectrum and total noise power in V_{out} for the circuit shown in Fig 6.a. 9 L4 CO2 PO2

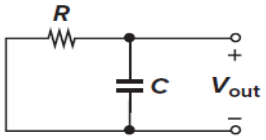

Fig. 6.a.

b. Draw the schematic of a 3-stage CMOS inverter ring oscillator and derive expression for its oscillation frequency considering (i) Small signal oscillations (ii) Large signal oscillations. Also illustrate how the inverter delay and number of stages can help in attaining required large signal frequency of oscillations. 9 L4 CO3 PO3

c. List and infer the significance of the following in Voltage Controlled Oscillator. (i) Center frequency (ii) Tuning range (iii) Supply and CMRR. 9 L4 CO3 PO3

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