



P.E.S. College of Engineering, Mandya - 571 401
 (An Autonomous Institution affiliated to VTU, Belagavi)
Eighth Semester, B.E. - Electronics and Communication Engineering
Semester End Examination; July - 2023
Algorithms for VLSI Physical Design

Time: 3 hrs

Max. Marks: 100

Course Outcomes

The Students will be able to:

CO1: To apply the knowledge of graph theory in VLSI Physical Design.

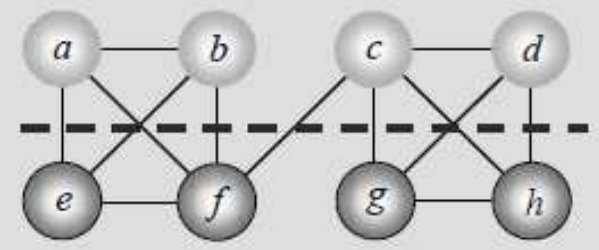
CO2: To be able to analyze the VLSI Physical Design algorithms.

CO3: To be able to apply the VLSI Physical Design algorithms.

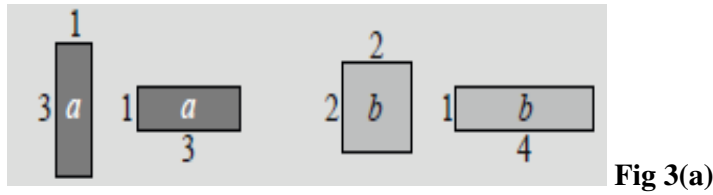
CO4: To be able to analyze the Physical Design for specific constraints.

Note: I) PART - A is compulsory. Two marks for each question.

II) PART - B: Answer any Two sub questions (from a, b, c) for a Maximum of 18 marks from each unit.

Q. No.	Questions	Marks	BLs	COs	POs
I : PART - A		10			
1 a.	Define cell based and array based in VLSI design styles.	2	L1	CO1	PO1
b.	Mention the optimization goals in floor planning.	2	L1	CO1	PO1
c.	Mention the steps in global routing flow.	2	L1	CO2	PO2
d.	Define channel routing.	2	L1	CO1	PO1
e.	List the timing driven placement in timing closure.	2	L1	CO4	PO1
II : PART - B		90			
UNIT - I		18			
2 a.	Briefly explain the steps of VLSI design flow in physical design.	9	L2	CO1	PO1
b.	Discuss the graph theory terminology.	9	L2	CO1	PO1
c.	Given the initial partition of nodes (a - h) as shown in Fig. 2(c) can be optimally partitioned using KL algorithm. Perform the first pass of the algorithm. The dotted line represents the initial partitioning.	9	L3	CO3	PO4
		Fig 2(c)			
UNIT - II		18			
3 a.	Given two blocks a and b are given along with their size options as shown in Fig. 3(a).				
i)	Determine the shape functions for each block a, b	9	L2	CO3	PO4

ii) Find the minimum area of the floor plan using both horizontal and vertical composition and its corresponding slicing tree



- b. Illustrate the pin assignment in chip planning. 9 L4 CO2 PO2
- c. Perform min-cut placement to place gates $a - f$ on a 2×4 grid as shown in Fig.3(c). Use Kernighan-Lin algorithms for Partitioning to find a placement with minimum wire length using alternating cutline direction.

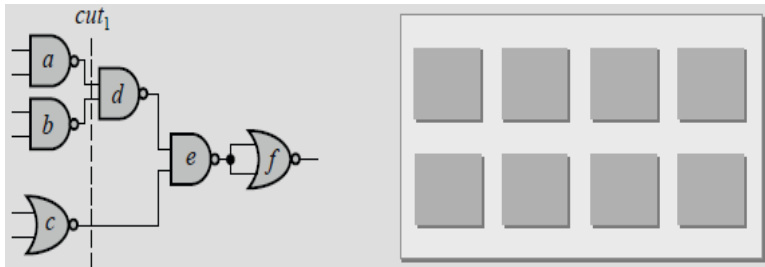


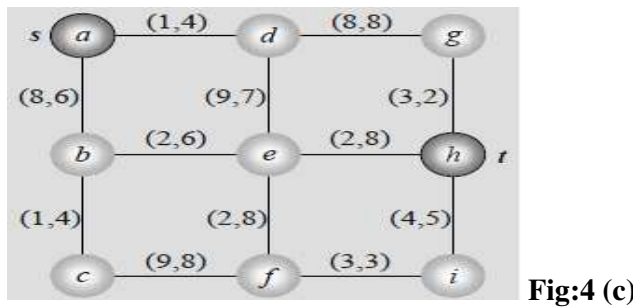
Fig: 3(c)

9 L4 CO3 PO5

UNIT - III

18

- 4 a. Discuss the quadratic and force-directed placement in analytic placement. 9 L2 CO2 PO2
- b. Explain the optimization goals in global routing. 9 L2 CO2 PO2
- c. For the graph with weights (w_1, w_2) as shown in Fig. 4(c), use Dijkstra's algorithm to find a minimum-cost path from the starting node $s = a$ to the target node $t = i$. Generate the tables for Groups 2 and 3.



UNIT - IV

18

- 5 a. **Given:** Channel routing instance as shown in Fig. 5(a). Perform the left-edge algorithm to route nets A-J in the channel.

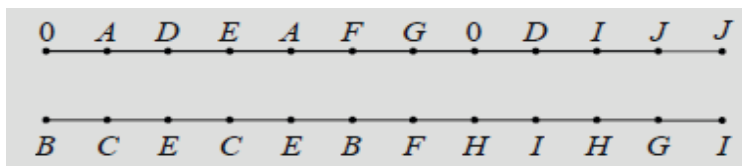


Fig: 5(a)

9 L4 CO3 PO5

b. Illustrate the over the cell routing algorithms in detailed routing.

9 L2 CO2 PO2

c. **Given:** Pins P1-P12.

P1 (2,17) P2 (1,14) P3 (11,15) P4 (4,11)

P5 (14,12) P6 (2, 9) P7 (11, 9) P8 (12, 6)

P9 (16, 6) P10 (7, 4) P11 (3, 1) P12 (14, 1) as shown in Fig. 5(c). Find a heuristic octilinear Steiner minimum tree.

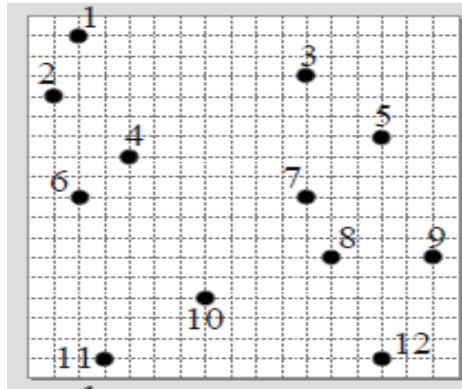


Fig:5(c)

9 L1 CO3 PO5

UNIT - V

18

6 a. Given the logic circuit shown in Fig. 6(a). Draw the timing graph and Determine the;

- i) AAT ii) RAT ii) Slack of each node

The AATs of the inputs are in angular brackets, the delays are in parentheses, and the RAT of the output is in square brackets.

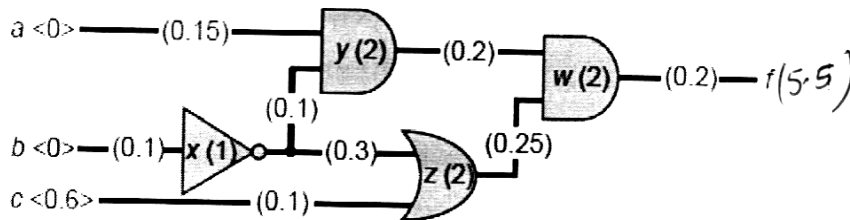


Fig:6(a)

9 L2 CO4 PO4

b. Illustrate the timing-driven routing in timing closure.

9 L4 CO4 PO1

c. Along with example, describe the gate sizing and buffering in physical synthesis.

9 L2 CO4 PO4

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